ST9 FAMILY
8/16 BIT MCU

PRODUCT OVERVIEW

1st EDITION

APRIL 1993

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED.

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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ST9 APPLICATION TAILORED MCU

The ST9 family of 8/16 bit Microcontrollers (MCUs) was designed after the requirements of the most advanced applications in computer, consumer, telecom, industrial and automotive Segments.

Processed with the same proprietary CMOS EPROM and EEPROM technologies that have established SGS-THOMSON as a world leading supplier of non-volatile memories, the ST9 provides high speed computing with reduced power consumption.

Built around a high performance, register based core, the ST9 family offers different program and data memory sizes and a wide range of on-chip peripherals to meet the needs of most systems.

Time to market is minimized with ST9's well defined, socket compatible, evolution path, from application evaluation with EPROMs, to prototyping using OTPs, up to the high volume production using cost effective ROM versions.

All standard ST9 devices include a Serial Peripheral Interface, a Watchdog Timer to ensure system integrity against externally generated malfunctions, bit configurable I/Os, prioritizable Interrupts for real-time data handling, and DMA for fast data transfers with handshake (HSHK).

In addition ST9 family variants include up to three Multi-Function Timers, two Serial Communication Interfaces (SCI), an Analog to Digital converter (A/D) and On-Screen Display and Data-Slicer for TV control.

REGISTER BASED ARCHITECTURE

The Register based architecture provides more efficient data handling and reduced code size compared to an accumulator based MCU. It also provides the capability for fast context switching.

224 of the 256 8-bit Registers in the ST9 Register File are available as accumulators, index registers, or stack pointers and can be cascaded to perform all these functions as 16-bit registers. The remaining registers are dedicated to system and peripheral control.

This architecture is common to all ST9 devices.

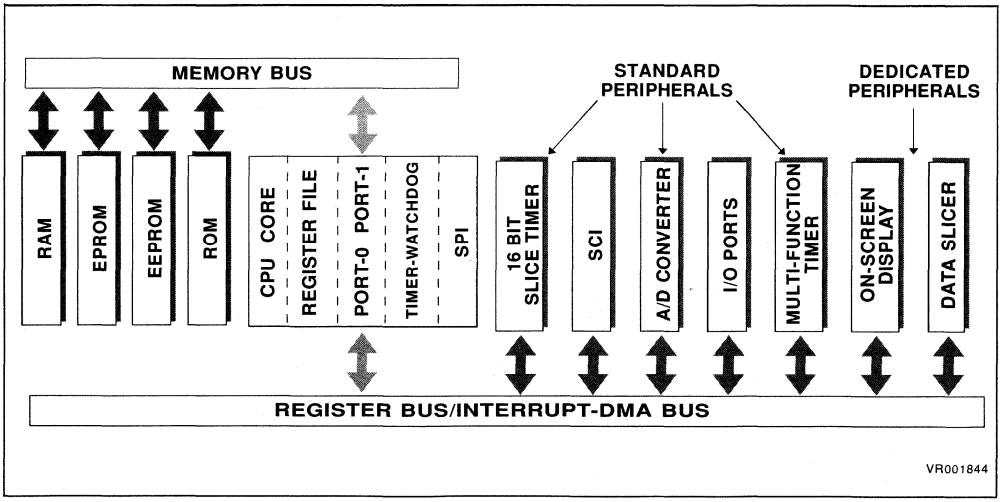
FLEXIBLE I/O

The flexibility of the ST9 I/O pins allow designers to match the MCU to the application, and not the application to the MCU.

Most I/Os can be individually programmed as input (TTL or CMOS thresholds), output (open-drain or push-pull), bidirectional, or as the Alternate Function of a peripheral, such as a Timer or an A/D Converter.

COMPREHENSIVE SCI

Serial communication is easily implemented, using formats and facilities offered by the ST9 Serial Communication Interface.



ST9 Architectural Block Diagram

INTRODUCTION

This peripheral provide full flexibility in character format (5,6,7,8 databits), odd, even or no parity, address bit, 1, 1.5, or 2 stop bits in asynchronous mode, and an integral baud rate generator allowing communication at up to 370k baud in asynchronous mode or 1.5Mbyte/s in synchronous mode.

Industrial, telecom and communication systems users can furthermore benefit from the self-test and address bit wake-up facility offered by the character search mode.

FAST A/D WITH ANALOG WATCHDOG

Up to 8 analog input voltages can be sequentially converted by the Analog to Digital converter including on-chip sample and hold.

The 11µs conversion time, and the possibility to trigger conversions either by the on-chip timers, or by external sources, allows real time processing of analog data.

CPU loading is also reduced by the analog watchdog on two channels, the peripheral interrupts the ST9 when the analog input voltage moves out of a preset threshold window.

UNIVERSAL SPI

A universal Serial Peripheral Interface, providing basic I^2C-bus, Microwire-Bus and S-BUS functionality, allows efficient communication with low-cost external peripherals or serial access memories such as EEPROMs.

MULTI-FUNCTION TIMERS

The 16 bit up/down counter operating in 13 modes gives the ST9 Multi-function Timer the possibility to cover most application timing requirements.

Two input pins, programmable as external clock, gate or trigger, allow 16 modes of operation, including auto-discrimination of the direction of externally generated signals.

Pulse Width Generation can easily be implemented, using the overflow/underflow signal and the two 16 bit comparison registers, each of them able to independently set, reset, toggle or ignore two output bits.

The Multifunction Timer outputs may also generate interrupts for system scheduling, and trigger DMA transactions of a data byte to or from a data table in memory through an I/O Port with handshake.

ON-SCREEN DISPLAY

Interactive information display for television control is easily implemented with the powerful ST9 On-Screen Display. With up to 34 characters in 15 rows, and colour, italic, underline, flash, tranparent and fringe options, the 128 character set can be adapted for all needs.

DATA-SLICER

Closed Caption Data can be easily extracted from the video signal with the ST9 Data Slicer. When used in conjunction with the ST9 On-Screen Display, a powerful TV controller can be achieved with the minimum of components.

POWERFUL INSTRUCTION SET

The ST9 has 14 addressing modes and instructions (including multiply, divide, table search and block move) to cover all data manipulation needs, bit, byte and word, at the speed required by even the most demanding control application.

Its instruction set was conceived to facilitate the software designer's task, and to improve programming efficiency.

FULL DEVELOPMENT SUPPORT

ST9 Development Tools are designed for application development efficiency.

A high level macro assembler (with IF/THEN, DO/WHILE, SYSTEM/CASE, PROCedure C language constructs in the assembler) is available, as well as an incremental linker able to link up to 16 Mbytes of program and data, a library maintainer for archiving common software routines and Software Simulation of the code execution, allowing off-line code development and timing analysis.

The validated ANSI standard C Compiler generates optimised code for the ST9. In addition a GNU C cross-compiler and Linker allows development support under the Microsoft Windows 3™ environment.

Cost effective emulation is provided either through a software module running on standard PCs, or with the ST9 Starter Kit, offering hardware emulation capability.

Full real time hardware emulation is provided by the ST9-HDS system.

ST9 FAMILY OVERVIEW

ST9 FAMILY OVERVIEW

All devices have 256 byte Register File with 224 General Purpose Registers (Accumulators/RAM), TWD and SPI Peripherals.

DEVICE	ROM x8	EPROM OTP ROM[1] x8	RAM x8	EEPROM x8	MFT	SCI	A/D Inputs	BSS	MAX I/O	HSHK
ST9026	16K		256		1	1			40	1
ST9027	16K		256		1	1			32	1
ST9028	16K		256		1	1			36	1
ST90E26		16K	256		1	1			40	1
ST90E27		16K	256		1	1			32	1
ST90E28		16K	256		1	1			36	1
ST90T26		16K[1]	256		1	1			40	1
ST90T27		16K[1]	256		1	1			32	1
ST90T28		16K[1]	256		1	1			36	1
ST90R26	-	-	256		1	1			32	1
ST9030	8K				2	1	8		56	1
ST90E30		8K			2	1	8		56	1
ST90T30		8K[1]			2	1	8		56	1
ST90R30	-	-			2	1	8		40	1
ST9032	12K	-			2	1	8		56	1
ST9036	16K		256		2	1	8		40	1
ST90E36		16K	256						40	
ST90T36		16K[1]	256						40	
ST9040	16K		256	512	2	1	8		56	1
ST90E40		16K	256	512	2	1	8		56	1
ST90T40		16K[1]	256	512	2	1	8		56	1
ST90R40	-	-	256	512	2	1	8		40	1
ST90R50	-	-			3	2	8	1	56	2
ST90R51	-	-			3	2	8	1	54	2
ST9054	32K		1280		3	2	8	1	72	2
ST90E54		32K	1280		3	2	8	1	72	2
ST90R54			1280		3	2	8	1	72	2
ST9292	24K		384				3[2]		41	
ST92E92		24K	384				3[2]		41	
ST92T92		24K[1]	384				3[2]		41	
ST9293	32K		640				4[2]		41	
ST92E93		32K	640				4[2]		41	
ST92T93		32K[1]	640				4[2]		41	

Keys :

TWD	Timer/Watchdog	SCI	Serial Communications Interface
SPI	Serial Peripheral Interface	A/D	8 bit 8 channel A/D Converter
MFT	Multi-Function Timer	BSS	Bankswitch logic 16M byte address range
I/O	In :TLL/CMOS, Out : OD/PP Alternate Functional Peripheral	HSHK	# Ports with Handshake Capability

Notes :

1. OTP ROM = One Time Programmable
2. 6 bit A/D Converter

DEVICE	OTHER FEATURES	PACKAGE (Operating temperature)			PAGE
		DIP	LCC	QFP	
ST9026		P48 (1,6)			9
ST9027		P40 (1,6)			9
ST9028			P44 (1,6)		9
ST90E26		C48W (1)			11
ST90E27		C40W (1)			11
ST90E28			C44W (1)		11
ST90T26		P48 (6)			11
ST90T27		P40 (6)			11
ST90T28			P44 (6)		11
ST90R26		P48 (6)			13
ST9030			P68 (1,6)	P80 (1)	15
ST90E30			C68W (1)	C80W (1)	17
ST90T30			P68 (6)	P80 (1)	17
ST90R30			P68 (6)		19
ST9032			P68 (1,6)	P80 (1)	21
ST9036			P68 (1,6)	P80 (1)	23
ST90E36			C68W (1)	C80W (1)	25
ST90T36			P68 (6)	P80 (1)	25
ST9040			P68 (1,6)	P80 (1)	27
ST90E40			C68W (1)	C80W (1)	29
ST90T40			P68 (6)	P80 (1)	29
ST90R40			P68 (6)		31
ST90R50			P84 (6)		33
ST90R51				P80 (1)	35
ST9054			P84 (1,6)		37
ST90E54			C84W (1)		39
ST90R54			P84 (6)		41
ST9292	} OSD, STM,	PS42 (1)			43
ST92E92	DSL, PWM	CS42W (1)			45
ST92T92		PS42 (1)			45
ST9293	} OSD, STM	PS42 (1)			47
ST92E93		CS42W (1)			49
ST92T93		PS42 (1)			49

Keys :

OSD	On Screen Display	Pxx	Plastic Package
STM	Slice Timer	PSxx	Plastic Shrink DIP Package
DSL	Data Slicer extracting Closed Caption Data	CxxW	Ceramic Package with window
PWM	Pulse Width Modulation outputs	CSxxW	Ceramic Shrink DIP Package with window

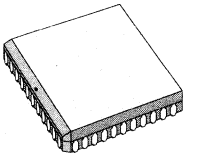
Temperature Ranges :

(1)One version available, 0 to +70°C (6)One version available, -40 to+85°C
(1,6)Two versions available, 0 to +70°C and -40 to+85°C

ST9026,ST9027,ST9028

16K ROM HCMOS MCUs WITH RAM

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 16K bytes of ROM,
  256 bytes of RAM,
  224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 48-pin Dual in Line Plastic package for ST9026
- 40-pin Dual in Line Plastic package for ST9027
- 44-lead Plastic Leaded Chip Carrier package for ST9028
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 40 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit Multifunction Timer, with an 8-bit prescaler and 13 operating modes
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases



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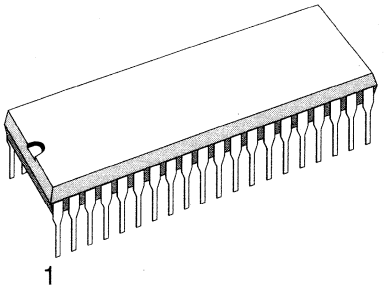

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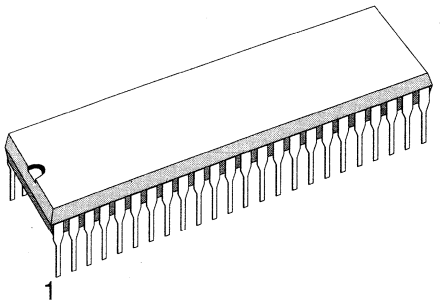


PDIP48

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST9026, ST9027 and ST9028 (following mentioned as ST902X) are ROM members of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 16K bytes of on-chip ROM, microcontrollers able to manage external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

The nucleus of the ST902X is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

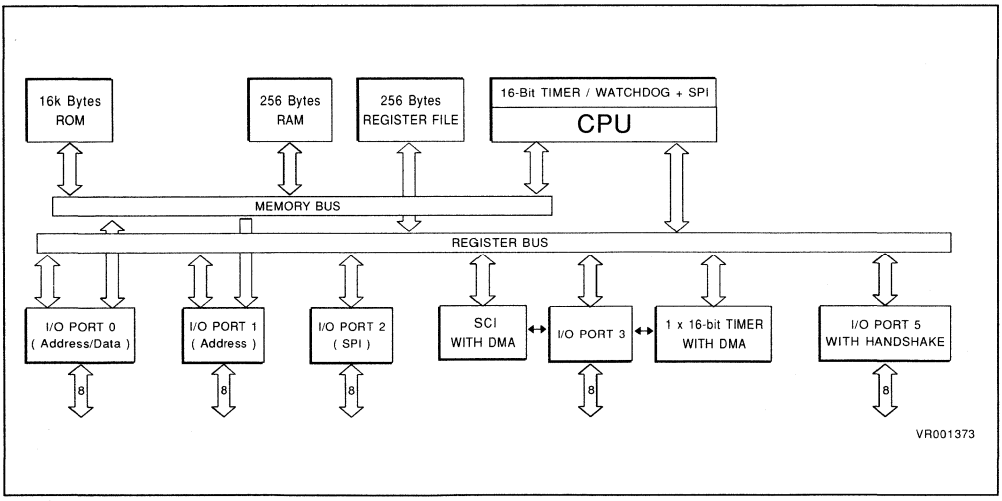
The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST902X with up to 40 I/O lines dedicated to digital Input/Output. These lines are grouped into up to five 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16 bit MultiFunction Timer, with an 8 bit Prescaler and 12 operating modes allows simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

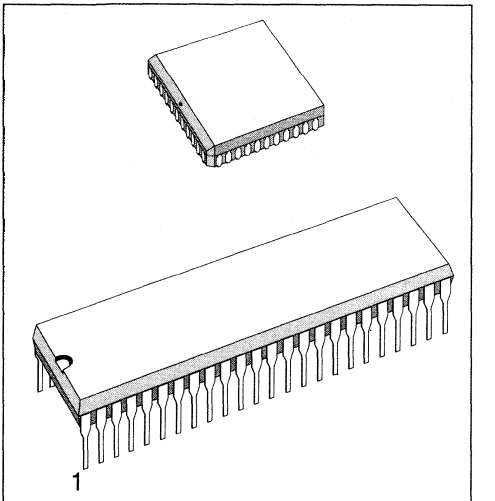
Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST902X Block Diagram



16K EPROM HCMOS MCUs WITH RAM

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 16K bytes of EPROM or OTP ROM
  256 bytes of RAM,
  224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 48-pin Window Dual in Line Ceramic Multilayer package for ST90E26
- 40-pin Window Dual in Line Ceramic Multilayer package for ST90E27
- 44-lead Window Ceramic Leaded Chip Carrier package for ST90E28
- 48-pin Dual in Line Plastic package for ST90T26
- 40-pin Dual in Line Plastic package for ST90T27
- 44-lead Plastic Leaded Chip Carrier package for ST90T28
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 40 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit Multifunction Timer, with an 8-bit prescaler and 13 operating modes
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9026/27/28 16K ROM device



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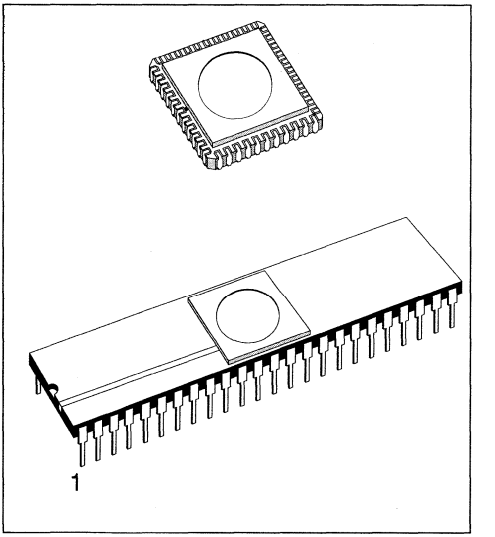


GENERAL DESCRIPTION

The ST90E26, ST90E27 and ST90E28, ST90T26, ST90T27 and ST90T28 (following mentioned as ST90E2X) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM ST90E2X can be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 16K bytes of on-chip ROM, microcontrollers able to manage external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

The nucleus of the ST90E2X is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

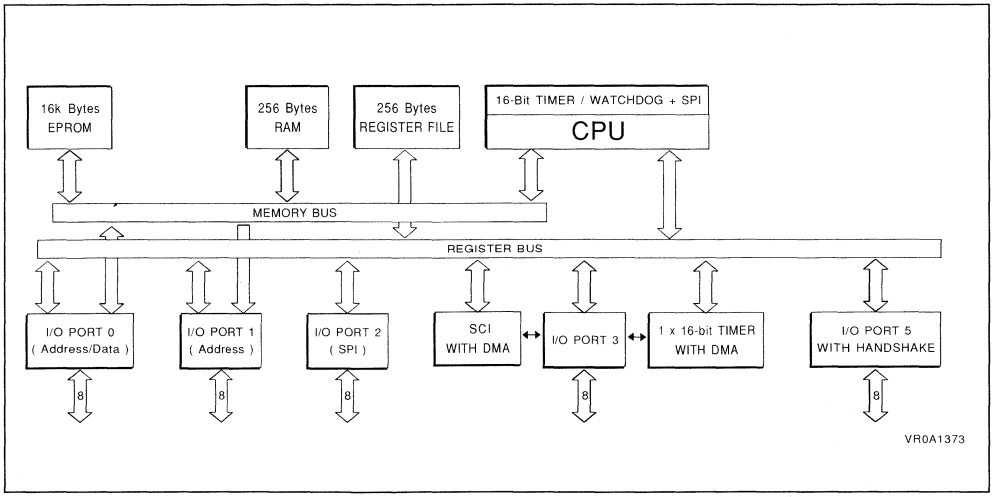
The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E2X with up to 40 I/O lines dedicated to digital Input/Output. These lines are grouped into up to five 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16 bit MultiFunction Timer, with an 8 bit Prescaler and 12 operating modes allows simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90E2X Block Diagram

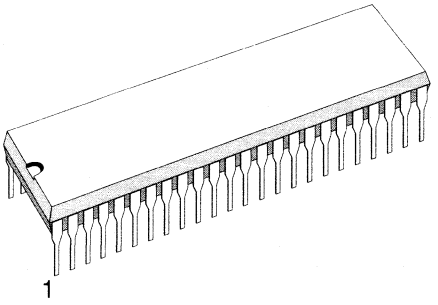


SGS-THOMSON MICROELECTRONICS

ST90R26

ROMLESS HCMOS MCU WITH RAM

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 256 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- Romless to allow maximum external memory capability
- 48-lead Plastic Dual in Line package for ST90R26
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 24 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit Multifunction Timer, with an 8-bit prescaler and 13 operating modes
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9026 16K ROM device (also available in windowed and One Time Programmable EPROM packages



PDIP48

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90R26 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ROMLESS ST90R26 can be configured as a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the ST90R26 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM-bus Interface, plus memory interface. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

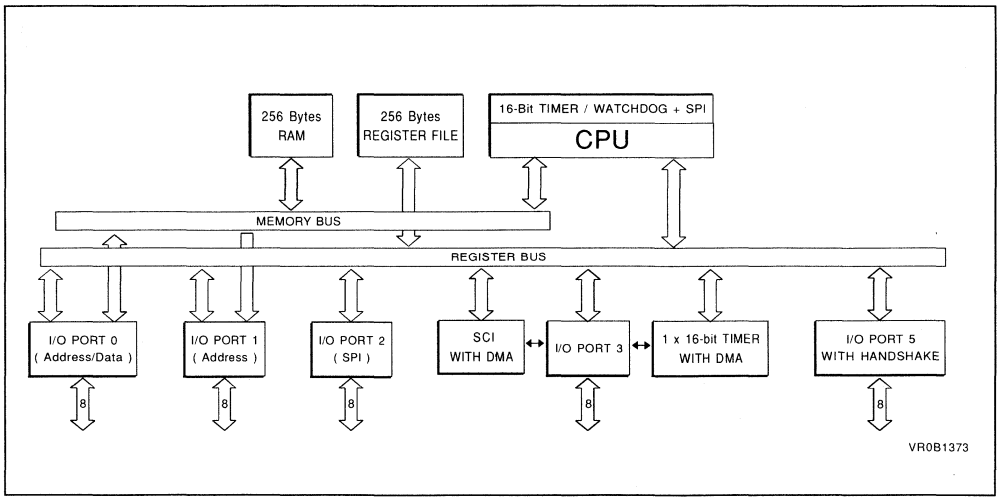
The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R26 with up to 32 I/O lines dedicated to digital Input/Output. These lines are grouped into up to four 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, address lines, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16 bit MultiFunction Timer, with an 8 bit Prescaler and 12 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90R26 Block Diagram

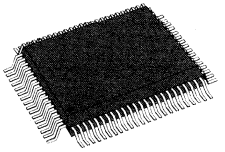


SGS-THOMSON MICROELECTRONICS

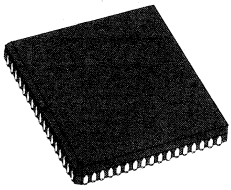
ST9030

8K ROM HCMOS MCU WITH A/D CONVERTER

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 8K bytes of ROM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 80-pin Plastic Quad Flat Pack package for ST9030Q
- 68-lead Plastic Leaded Chip Carrier package for ST9030C
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases



PQFP80



PLCC68

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST9030 is ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM part is fully compatible with its EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as standalone microcontrollers with 8K bytes of on-chip ROM, microcontrollers able to manage external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

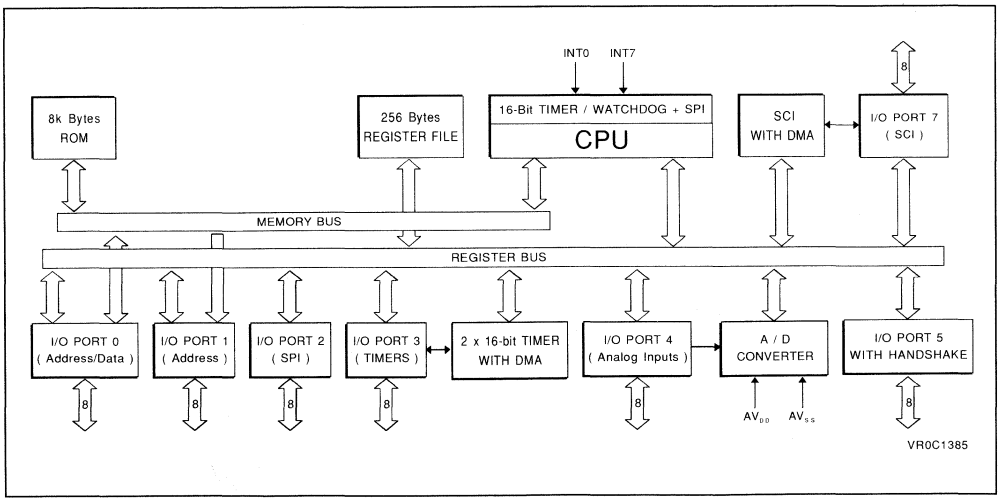
The nucleus of the ST9030 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM BUS Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9030 with 56 I/O lines dedicated to digital Input/Output. These lines are grouped into seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit 1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST9030 Block Diagram

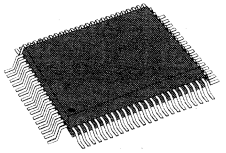


SGS-THOMSON MICROELECTRONICS

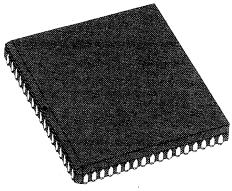
ST90E30
ST90T30

8K EPROM HCMOS MCUs WITH A/D CONVERTER

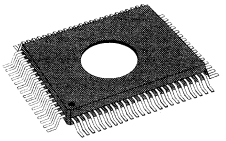
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 8K bytes of EPROM or OTP ROM 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 80-pin Plastic Quad Flat Pack package for ST90T30Q
- 68-lead Plastic Leaded Chip Carrier package for ST90T30C
- 80-pin Window Ceramic Quad Flat Pack package for ST90E30G
- 68-lead Window Ceramic Leaded Chip Carrier package for ST90E30L
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9030 8K ROM device



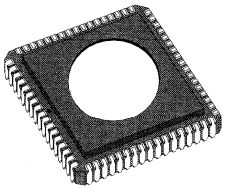
PQFP80



PLCC68



CQFP80W



CLCC68W

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90E30 and ST90T30 (following mentioned as ST90E30) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM ST90E30 may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 8K bytes of on-chip ROM, microcontrollers able to manage external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

The nucleus of the ST90E30 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C Bus and IM BUS Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E30 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

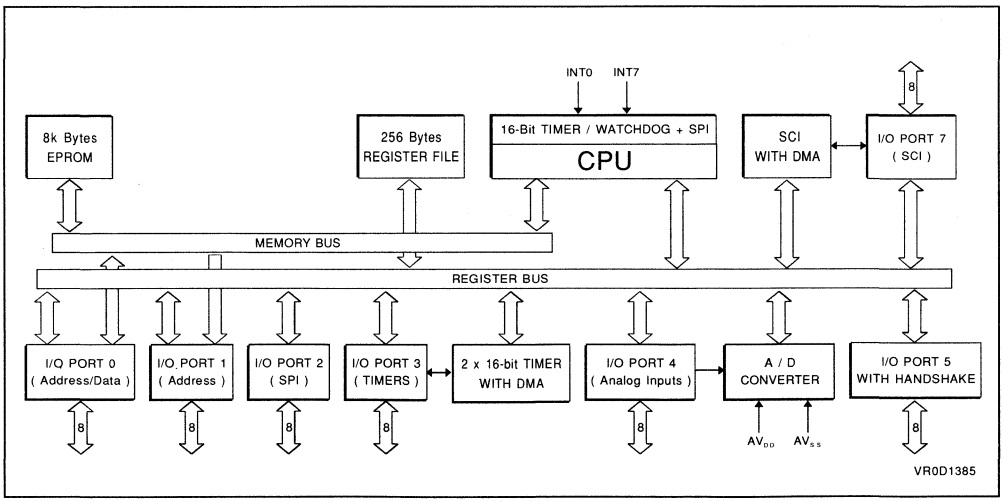
Three memory spaces are available: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90E30 Block Diagram



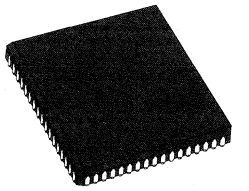
SGS-THOMSON MICROELECTRONICS

ST90R30

ROMLESS HCMOS MCU WITH A/D CONVERTER

ADVANCE DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- Romless to allow maximum external memory capability
- 68-lead Plastic Leaded Chip Carrier package
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 40 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9030 8K ROM device (also available in windowed and One Time Programmable EPROM packages)



PLCC68

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90R30 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ROMLESS ST90R30 can be configured as a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the ST90R30 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM-bus Interface, plus memory interface. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R30 with up to 40 I/O lines dedicated to digital Input/Output. These lines are grouped into up to five 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

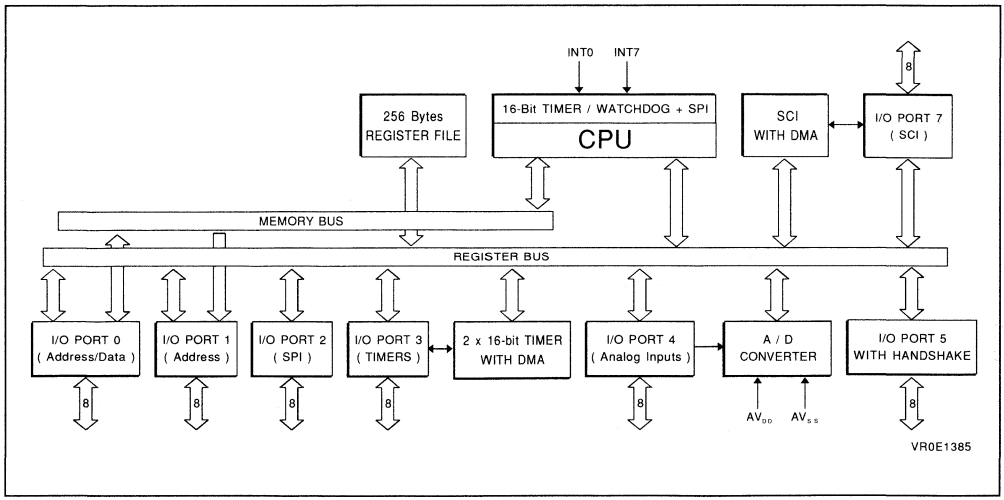
Three memory spaces are available: Program Memory (external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90R30 Block Diagram



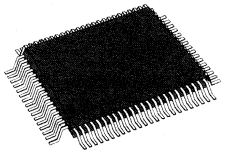
SGS-THOMSON MICROELECTRONICS

ST9032

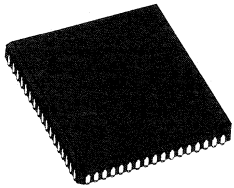
12K ROM HCMOS MCU WITH A/D CONVERTER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 12K bytes of ROM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 80-pin Plastic Quad Flat Pack package for ST9032Q
- 68-lead Plastic Leaded Chip Carrier package for ST9032C
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases
- Upward compatible with ST9030



PQFP80



PLCC68

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST9032 device are ROM members of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

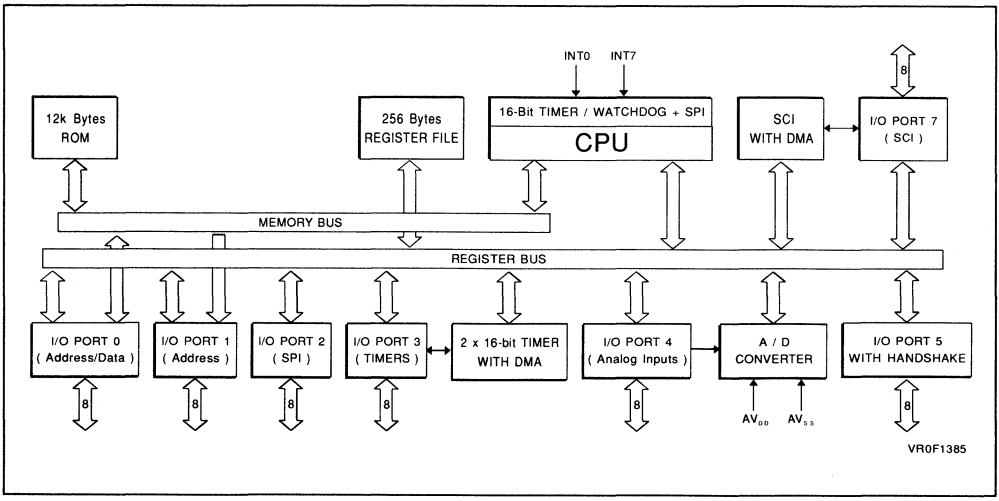
The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as standalone microcontrollers with 12K bytes of on-chip ROM, microcontrollers able to manage external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

The nucleus of the ST9032 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C Bus and IM BUS Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9032 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.
Three memory spaces are available: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST9032 Block Diagram



SGS-THOMSON MICROELECTRONICS

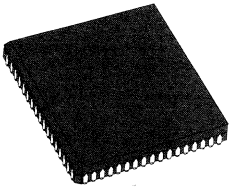
ST9036

16K ROM HCMOS MCU WITH RAM AND A/D CONVERTER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 16K bytes of ROM,
  256 bytes of RAM,
  224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 80-pin Plastic Quad Flat Pack package for ST9036Q
- 68-lead Plastic Leaded Chip Carrier package for ST9036C
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 72 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases
- Upward compatible with ST9030 and ST9032

PQFP80



PLCC68

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST9036 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM device is fully compatible with the EPROM version (ST90E36), which may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip ROM, a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the ST9036 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9036 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

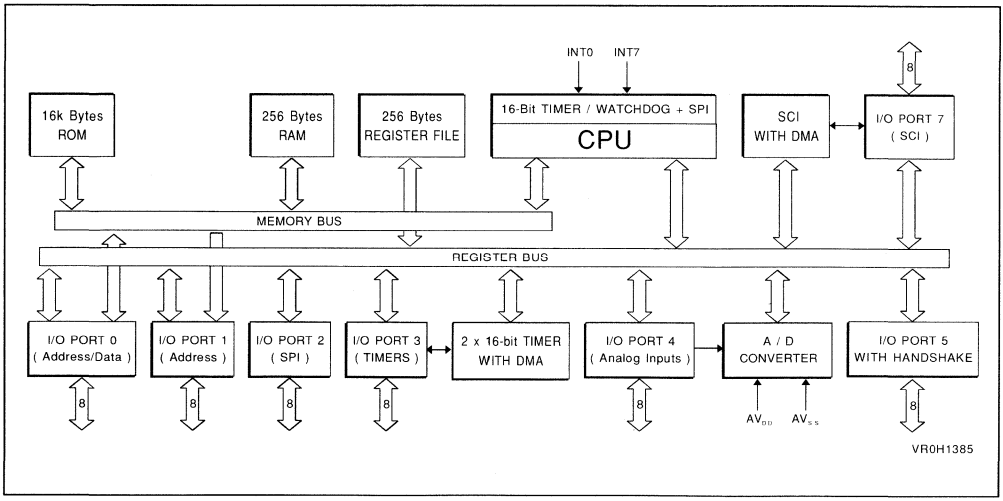
Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST9036 Block Diagram



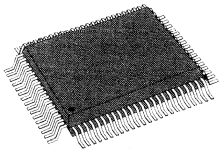
SGS-THOMSON MICROELECTRONICS

ST90E36
ST90T36

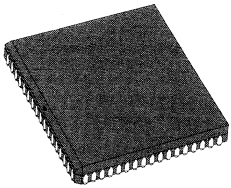
16K EPROM HCMOS WITH RAM AND A/D CONVERTER

PRELIMINARY DATA

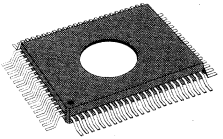
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 16K bytes of EPROM or OTP ROM, 256 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 80-pin Plastic Quad Flat Pack package for ST90T36Q
- 80-pin Window Ceramic Quad Flat Pack package for ST90E36G
- 68-lead Plastic Leaded Chip Carrier package for ST90T36C
- 68-lead Window Ceramic Leaded Chip Carrier package for ST90E36L
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9036 16K ROM device



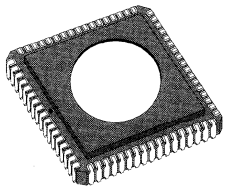
PQFP80



PLCC68



CQFP80W



CLCC68W

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90E36 and ST90T36 (following mentioned as ST90E36) are EPROM and OTP members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM ST90E36 may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 16K bytes of on-chip ROM, microcontrollers able to manage external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

The nucleus of the ST90E36 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C Bus and IM BUS Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E36 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

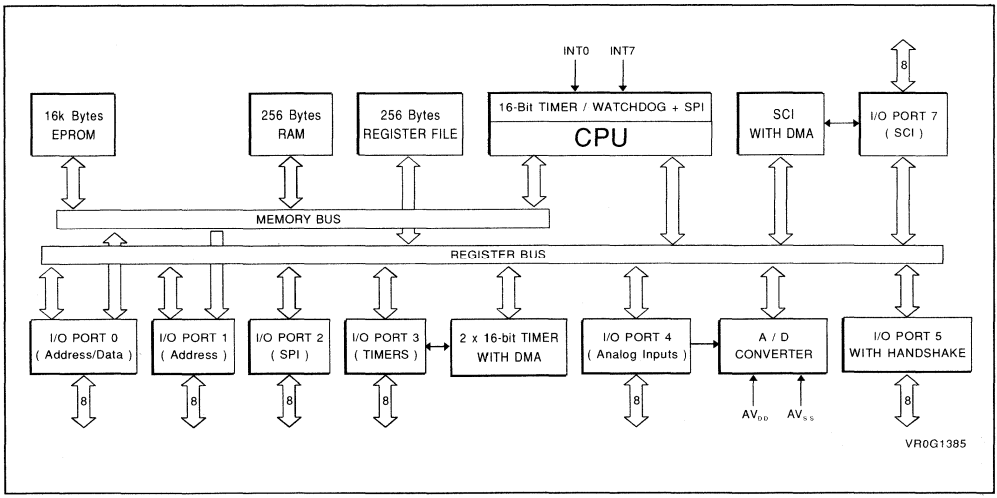
Three memory spaces are available: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90E36 Block Diagram

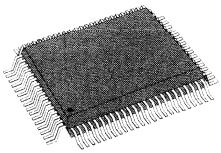


SGS-THOMSON MICROELECTRONICS

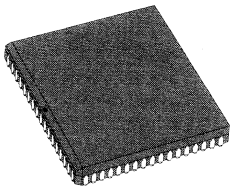
ST9040

16K ROM HCMOS MCU WITH EEPROM RAM AND A/D CONVERTER

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 16K bytes of ROM,
  256 bytes of RAM,
  224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 512 bytes EEPROM
- 80-pin PQFP package for ST9040Q
- 68-lead PLCC package for ST9040C
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases
- Upward compatible with ST9030, ST9032 and ST9036



PQFP80



PLCC68

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST9040 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM device is fully compatible with its EPROM version, which may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip ROM, a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

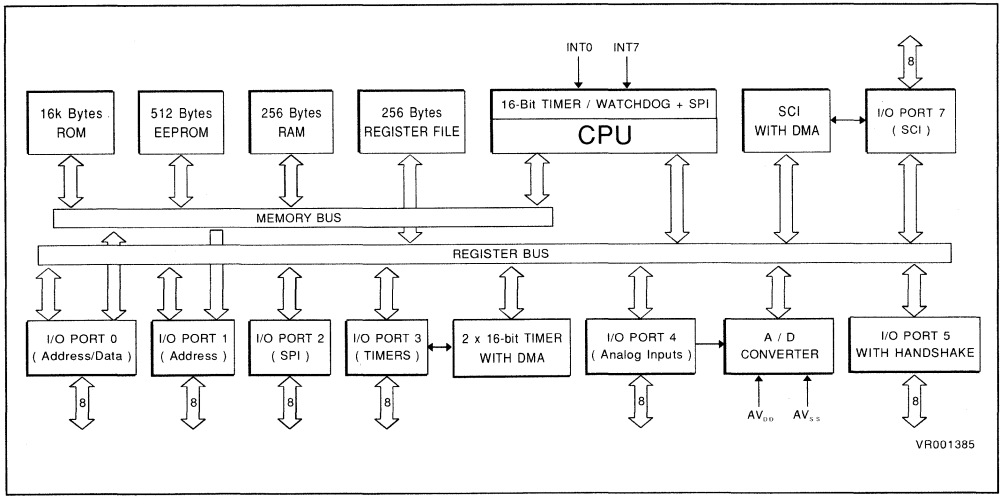
The nucleus of the ST9040 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9040 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST9040 Block Diagram

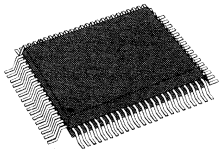


SGS-THOMSON MICROELECTRONICS

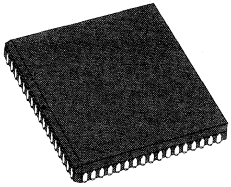
ST90E40
ST90T40

16K EPROM HCMOS MCU WITH EEPROM, RAM AND A/D CONVERTER

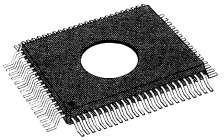
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 16K bytes of EPROM or OTP ROM, 256 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 512 bytes of EEPROM
- 80-pin Plastic Quad Flat Pack package for ST90T40Q
- 80-pin Window Ceramic Quad Flat Pack package for ST90E40G
- 68-lead Plastic Leaded Chip Carrier package for ST90T40C
- 68-lead Window Ceramic Leaded Chip Carrier package for ST90E40L
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9040 16K ROM device



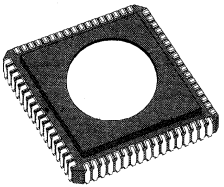
PQFP80



PLCC68



CQFP80W



CLCC68W

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90E40 and ST90T40 (following mentioned as ST90E40) are EPROM and OTP members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.

The EPROM ST90E40 may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip ROM, a microcontroller able to manage of external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the ST90E40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

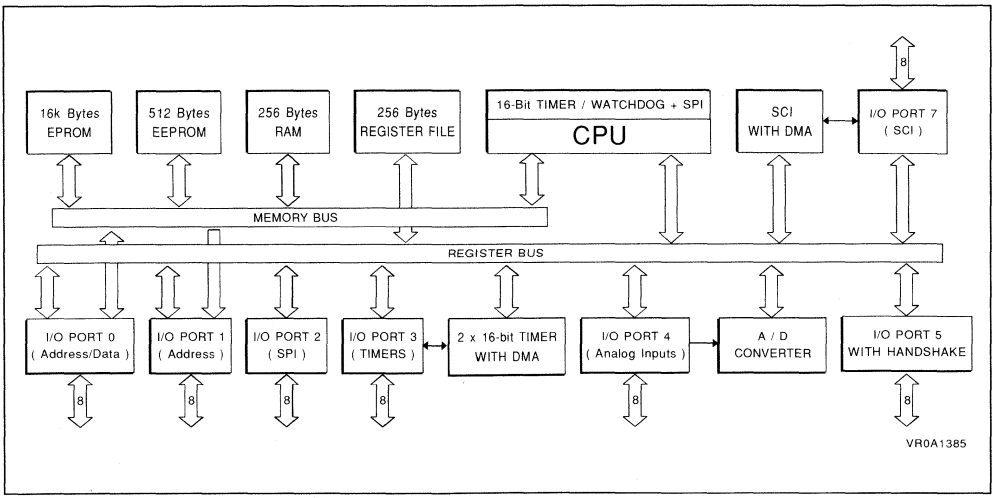
The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E40 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90E40 Block Diagram

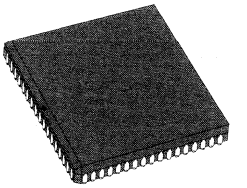


SGS-THOMSON MICROELECTRONICS

ST90R40

ROMLESS HCMOS MCU WITH EEPROM, RAM AND A/D CONVERTER

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 256 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- Romless to allow maximum external memory capbility
- 512 bytes EEPROM
- 68-lead Plastic Leaded Chip Carrier package
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 40 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9040 16K ROM device (also available in windowed and One Time Programmable EPROM packages)



PLCC68

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90R40 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ROMLESS ST90R40 can be configured as a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the ST90R40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM-bus Interface, plus memory iinterface. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

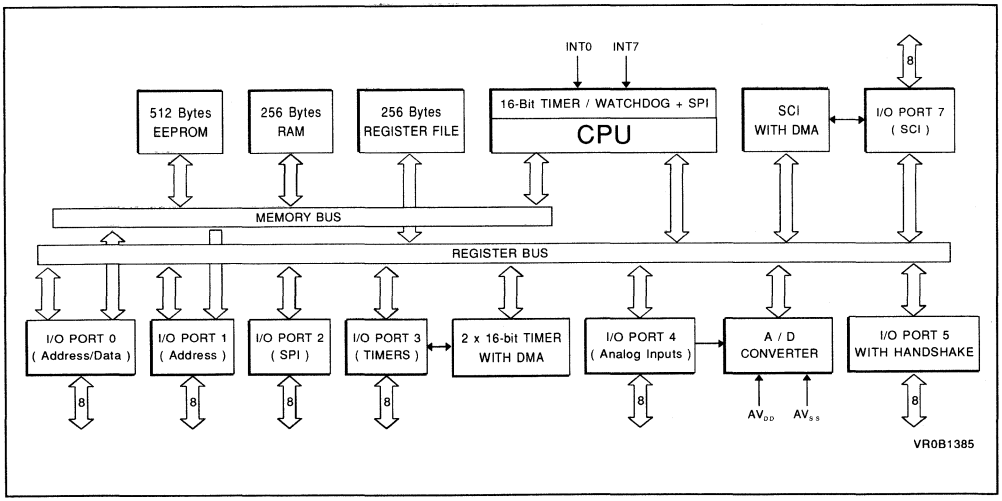
The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R40 with up to 40 I/O lines dedicated to digital Input/Output. These lines are grouped into up to five 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90R40 Block Diagram

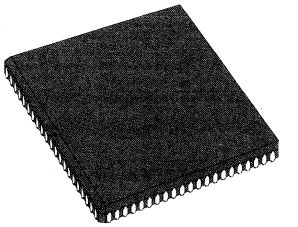


SGS-THOMSON MICROELECTRONICS

ST90R50

ROMLESS HCMOS MCU WITH BANKSWITCH AND A/D CONVERTER

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- Romless to allow maximum external memory flexibility in development and production phases
- Bankswitch logic allowing a maximum addressing capability of 8Mbytes for Program and Dataspace (16Mbytes total)
- 84-pin Plastic Leaded Chip Carrier package
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Three 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Two Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9054, 32K ROM device (also available in windowed and one time programmable EPROM packages)



PLCC84

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90R50 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems with its 16M byte addressing space when using the Bankswitch memory expansion.

The nucleus of the ST90R50 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus memory interface. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

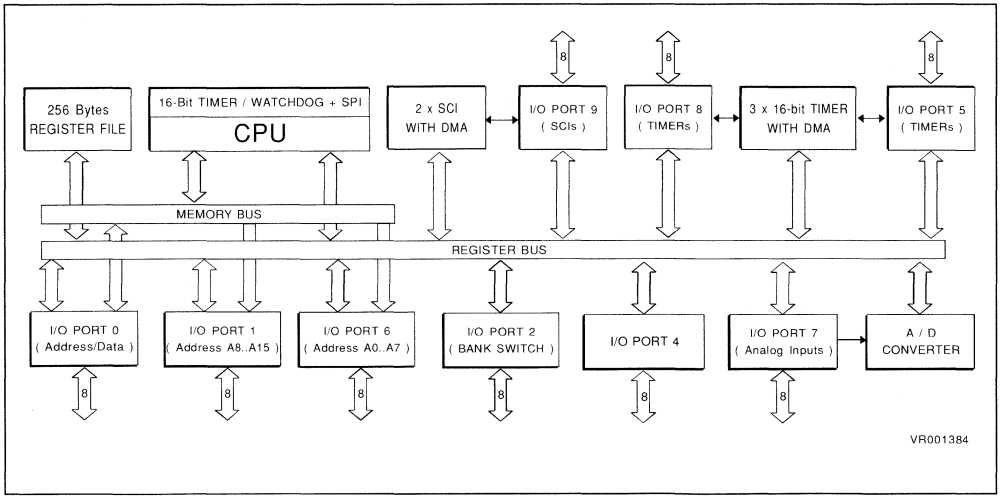
The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R50 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Completing the device are two full duplex Serial Communications Interfaces, each with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90R50 Block Diagram



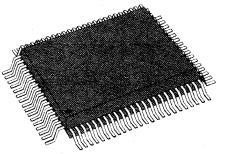
SGS-THOMSON MICROELECTRONICS

ST90R51

ROMLESS HCMOS MCU WITH BANKSWITCH

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- Romless to allow maximum external memory capability
- Bankswitch logic allowing a maximum addressing capability of 8Mbytes for Program and Dataspace (16Mbytes total)
- 80-pin Plastic Quad Flat Pack package
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 54 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Three 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- Two Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System



PQFP80

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90R51 is a Romless member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

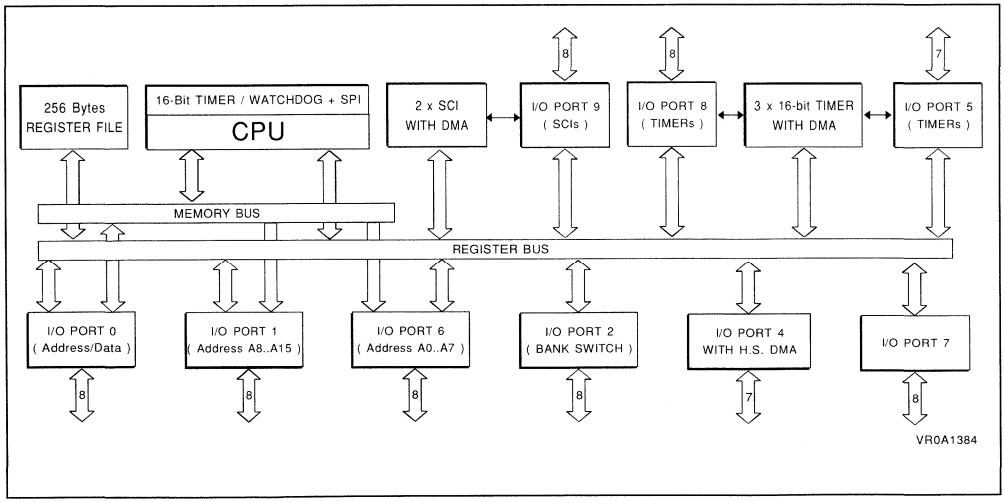
The Romless part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility

The nucleus of the ST90R51 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus memory interface. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R51 with up to 54 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.
Three basic memory spaces are available to support this wide range of configurations: Program Memory , Data Memory and the internal Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device are 2 full duplex Serial Communications Interfaces with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90R51 Block Diagram



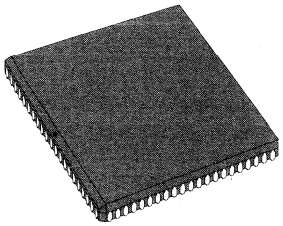
SGS-THOMSON MICROELECTRONICS

ST9054

32K ROM HCMOS MCU WITH BANKSWITCH AND A/D CONVERTER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 32K bytes of ROM,
  1280 bytes of RAM,
  224 general purpose registers available as RAM, accumulators or index registers (Register File)
- Bankswitch logic allowing a maximum addressing capability of 8Mbytes for Program and Dataspace (16Mbytes total)
- 84-pin Plastic Leaded Chip Carrier package
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 72 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Three 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Two Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases



PLCC84

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST9054 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM part is fully compatible with its EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 32K bytes of on-chip ROM, microcontrollers able to manage external memory (16M byte with the Bankswitch logic), or as parallel processing elements in a system with other processors and peripheral controllers.

The nucleus of the ST9054 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9054 with up to 72 I/O lines dedicated to digital Input/Output. These lines are grouped into up to nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, address and data buses for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

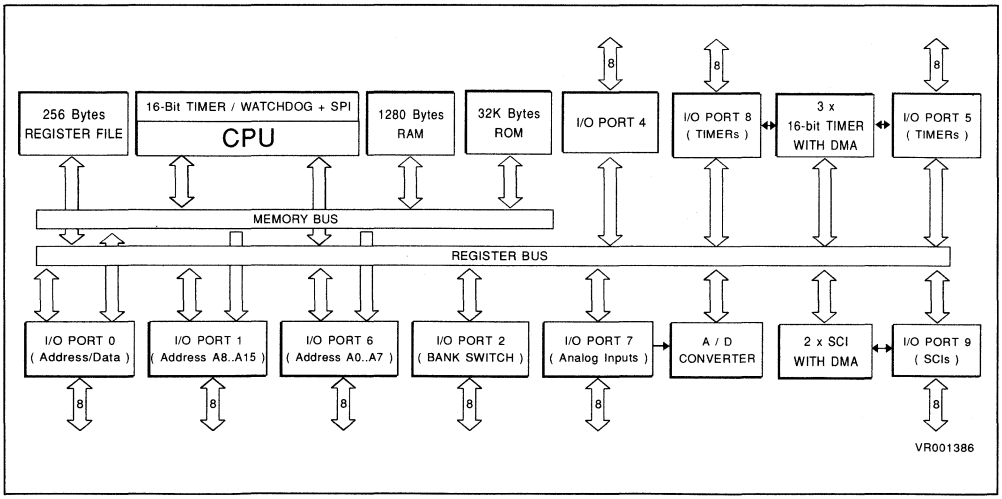
Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device are two full duplex Serial Communications Interfaces, each with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST9054 Block Diagram



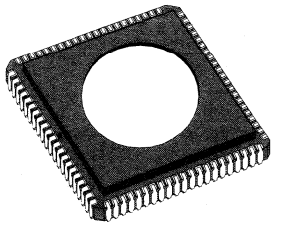
SGS-THOMSON MICROELECTRONICS

ST90E54

32K EPROM HCMOS MCU WITH BANKSWITCH AND A/D CONVERTER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 32K bytes of EPROM
  1280 bytes of RAM,
  224 general purpose registers available as RAM, accumulators or index registers (Register File)
- Bankswitch logic allowing a maximum addressing capability of 8Mbytes for Program and Dataspace (16Mbytes total)
- 84-pin Window Ceramic Leaded Chip Carrier package
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 72 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Three 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Two Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9054 32K ROM device



CLCC84W

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90E54 is an EPROM member of the ST9 family of microcontrollers, in windowed ceramic package , completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM ST90E54 may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 32K bytes of on-chip EPROM, microcontrollers able to manage external memory (16M byte with the Bankswitch logic), or as parallel processing elements in a system with other processors and peripheral controllers.

The nucleus of the ST90E54 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E54 with up to 72 I/O lines dedicated to digital Input/Output. These lines are grouped into up to nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, address and data buses for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

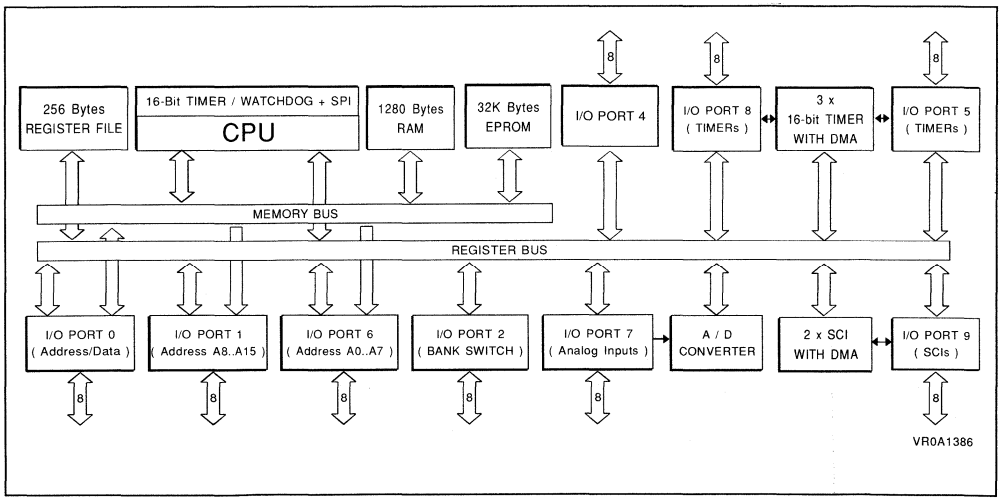
Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device are two full duplex Serial Communications Interfaces, each with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90E54 Block Diagram



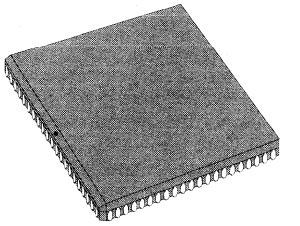
SGS-THOMSON MICROELECTRONICS

ST90R54

ROMLESS HCMOS MCU WITH BANKSWITCH AND A/D CONVERTER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 1280 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- Romless to allow maximum external memory flexibility in development and production phases
- Bankswitch logic allowing a maximum addressing capability of 8Mbytes for Program and Dataspace (16Mbytes total)
- 84-pin Plastic Leaded Chip Carrier package
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Three 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Two Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9054, 32K ROM device (also available in windowed EPROM packages)



PLCC84

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST90R54 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems with its 16M byte addressing space when using the Bankswitch memory expansion.

The nucleus of the ST90R54 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus memory interface. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R54 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

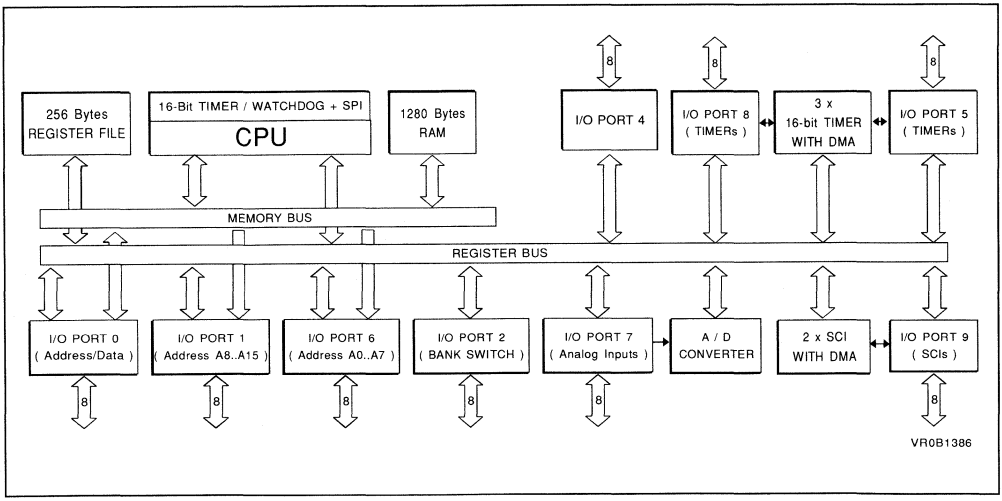
Three basic memory spaces are available to support this wide range of configurations: Program Memory (external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device are two full duplex Serial Communications Interfaces, each with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1. ST90R54 Block Diagram



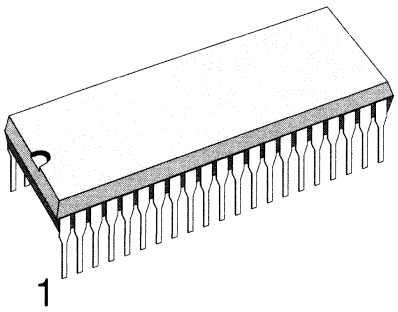
SGS-THOMSON MICROELECTRONICS

ST9292

24K ROM HCMOS MCU WITH ON SCREEN DISPLAY AND CLOSED CAPTION DATA SLICER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 24K bytes of ROM,
  384 bytes of RAM,
  224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead Shrink DIP package
- Interrupt handler and Serial Peripheral Interface as standard features
- 31 fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, flash, transparent and fringe attribute options
- Digital Data Slicer extracting closed caption data from video
- 8 8-bit PWM D/A outputs with repetition frequency 2 to 32kHz and 12V Open Drain Capability
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 3 channel Analog to Digital Converter, with integral sample and hold, fast 5.75µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed EPROM parts available for prototyping and pre-production development phases



PSDIP42

(Ordering Information at the end of the Datasheet)

DEVICE SUMMARY

Device	RAM	ROM
ST9292J4	384 bytes	16Kbytes
ST9292J5	384 bytes	24Kbytes

GENERAL DESCRIPTION

The ST9292 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 24K bytes of on-chip ROM.

The nucleus of the ST9292 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9292 with up to 31 I/O lines dedicated to digital Input/Output. These lines are grouped into up to six I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, address and data buses for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler.

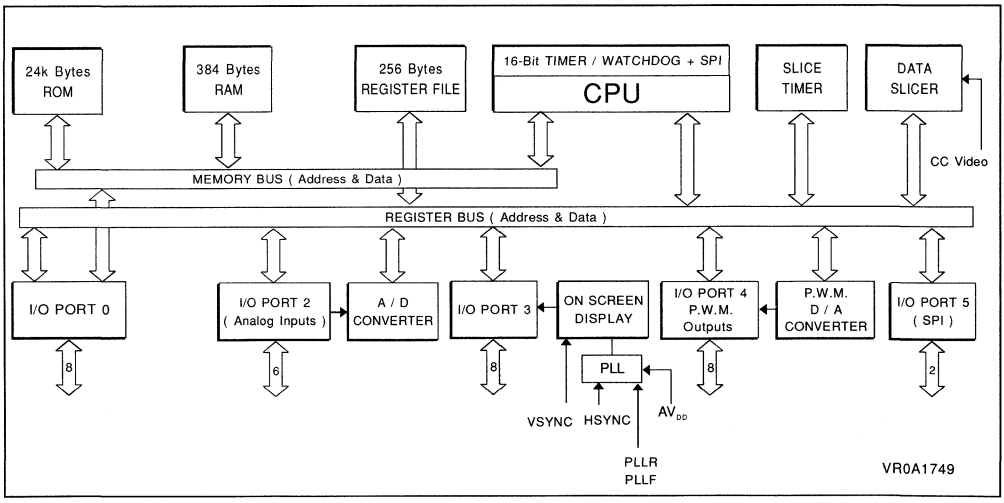
The human interface is provided by the On Screen Display module, this can produce up to 15 lines of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

Closed Caption control for the display of information transmitted through the video input is facilitated with the Data Slicer. This module has manual and automatic Slicing levels for both Sync and Data and allows the user to select the video line containing the data relative to the Vertical synchronisation pulse.

Control of TV settings is able to be made with up to eight 8-bit PWM outputs, with a frequency maximum of 23,437Hz at 8-bit resolution (INTCLK = 12MHz). Low resolutions with higher frequency operation can be programmed.

In addition there is a 3 channel Analog to Digital Converter with integral sample and hold, fast 5.75µs conversion time and 6-bit guaranteed precision.

Figure 1. ST9292 Block Diagram



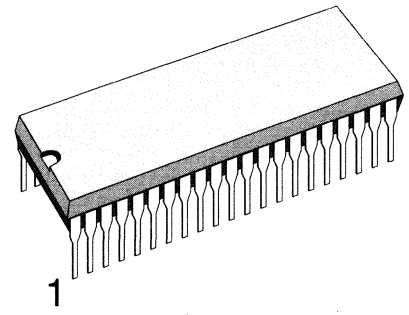
SGS-THOMSON MICROELECTRONICS

ST92E92
ST92T92

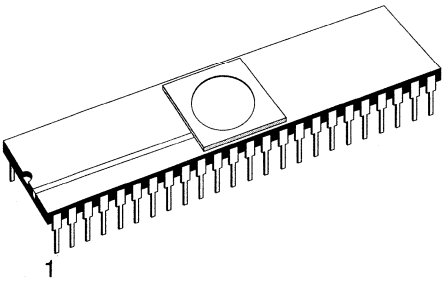
24K EPROM HCMOS MCU WITH ON SCREEN DISPLAY AND CLOSED-CAPTION DATA SLICER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 24K bytes of EPROM or OTP ROM, 384 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead Plastic Shrink DIP package for ST92T92
- 42-lead Window Ceramic Shrink DIP package for ST92E92
- Interrupt handler and Serial Peripheral Interface as standard features
- 31 fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, Flash, transparent and fringe attribute options
- Digital Data Slicer extracting closed caption data from video
- 8 8-bit PWM D/A outputs with repetition frequency 2 to 32kHz and 12V Open Drain Capability
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 3 channel Analog to Digital Converter, with integral sample and hold, fast 5.75µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9292 24K ROM device



PSDIP42



CSDIP42W

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST92E92 and ST92T92 are EPROM member of the ST9 family of microcontrollers in windowed Ceramic (E) and Plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM parts are fully compatible with their ROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 24K bytes of on-chip EPROM, microcontrollers able to manage up to 64K bytes of external memory.

The nucleus of the ST92E92 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST92E92 with up to 31 I/O lines dedicated to digital Input/Output. These lines are grouped into up to five I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler.

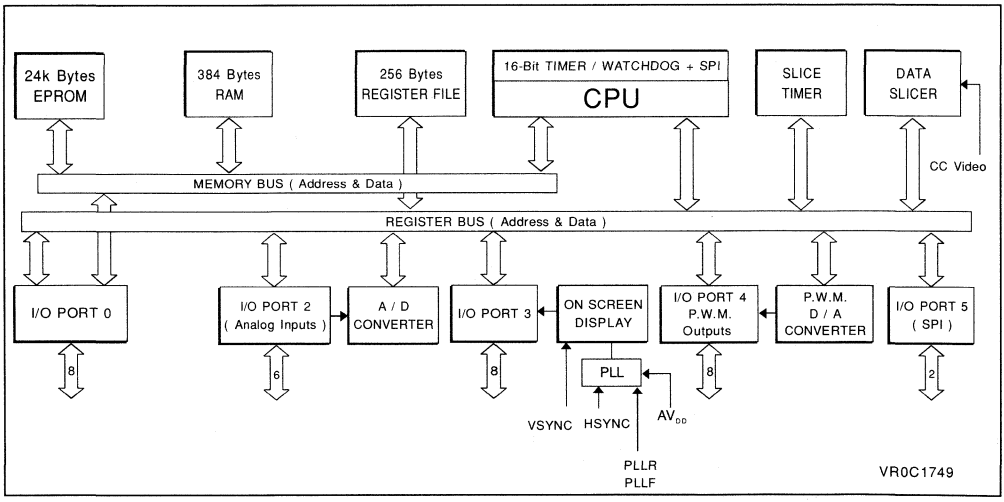
The human interface is provided by the On Screen Display module, this can produce up to 15 lines of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

Closed Caption control for the display of information transmitted through the video input is facilitated with the Data Slicer. This module has manual and automatic Slicing levels for both Sync and Data and allows the user to select the video line containing the data relative to the Vertical synchronisation pulse.

Control of TV settings is able to be made with up to eight 8-bit PWM outputs, with a frequency maximum of 23,437Hz at 8-bit resolution (INTCLK = 12MHz). Low resolutions with higher frequency operation can be programmed.

In addition there is a 3 channel Analog to Digital Converter with integral sample and hold, fast 5.75µs conversion time and 6-bit guaranteed resolution.

Figure 1. ST92E92 Block Diagram



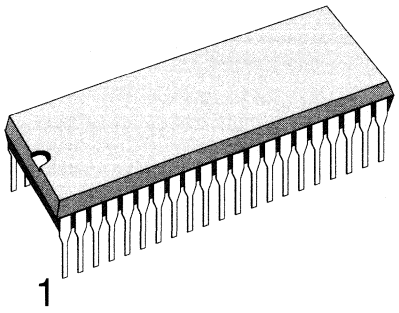
SGS-THOMSON MICROELECTRONICS

ST9293

32K ROM HCMOS MCUs WITH ON SCREEN DISPLAY AND A/D CONVERTER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 32K bytes of ROM,
  640 bytes of RAM,
  224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead Shrink DIP package
- Interrupt handler and Serial Peripheral Interface as standard features
- 31 fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, Flash, transparent and fringe attribute options
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 4 channel Analog to Digital Converter, with integral sample and hold, fast 5.5µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed EPROM parts available for prototyping and pre-production development phases



PSDIP42

(Ordering Information at the end of the Datasheet)

DEVICE SUMMARY

Device	RAM	ROM
ST9293J4	640 bytes	16Kbytes
ST9293J5	640 bytes	24Kbytes
ST9293J6	640 bytes	32Kbytes

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST9293 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 32K bytes of on-chip ROM.

The nucleus of the ST9293 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9293 with up to 31 I/O lines dedicated to digital Input/Output.

These lines are grouped into up to five I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

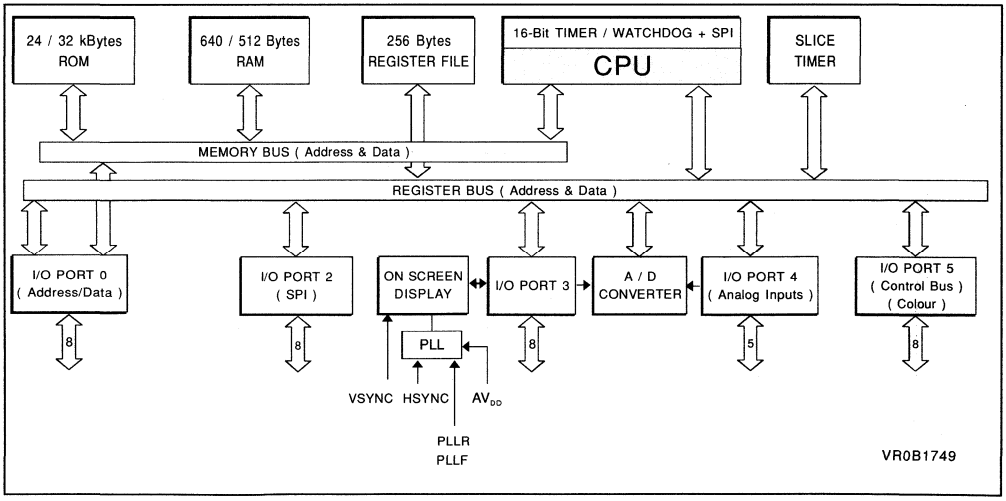
Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler and 6 operating modes allows simple use for waveform generation and measurement, PWM functions and many other system timing functions.

The human interface is provided by the On Screen Display module, this can produce up to 15 lines of of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

In addition there is a 4 channel Analog to Digital Converter with integral sample and hold, fast 5.5µs conversion time and 6-bit guaranteed precision.

Figure 1. ST9293 Block Diagram



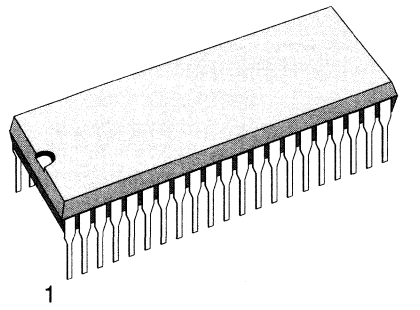
SGS-THOMSON MICROELECTRONICS

ST92E93
ST92T93

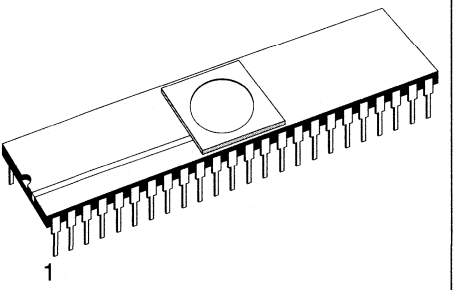
32K EPROM HCMOS MCUs WITH ON SCREEN DISPLAY AND A/D CONVERTER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 32K bytes of EPROM or OTP ROM, 640 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead Plastic Shrink DIP package for ST92T93
- 42-lead Window Ceramic Shrink DIP package for ST92E93
- Interrupt handler and Serial Peripheral Interface as standard.features
- 31 fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, Flash, transparent and fringe attribute options
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 4 channel Analog to Digital Converter, with integral sample and hold, fast 5.5µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating SystemCompatible with ST9293 32K ROM device



PSDIP42



CSDIP42W

(Ordering Information at the end of the Datasheet)

January 1993

This is short overview of an ST9 Family Member. Please contact SGS-THOMSON for further information.

GENERAL DESCRIPTION

The ST92E93 and ST92T93 are EPROM member of the ST9 family of microcontrollers in windowed Ceramic (E) and Plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM parts are fully compatible with their ROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 32K bytes of on-chip EPROM.

The nucleus the ST92E93 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST92E93 with up to 31 I/O lines dedicated to digital Input/Output.

These lines are grouped into up to five I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

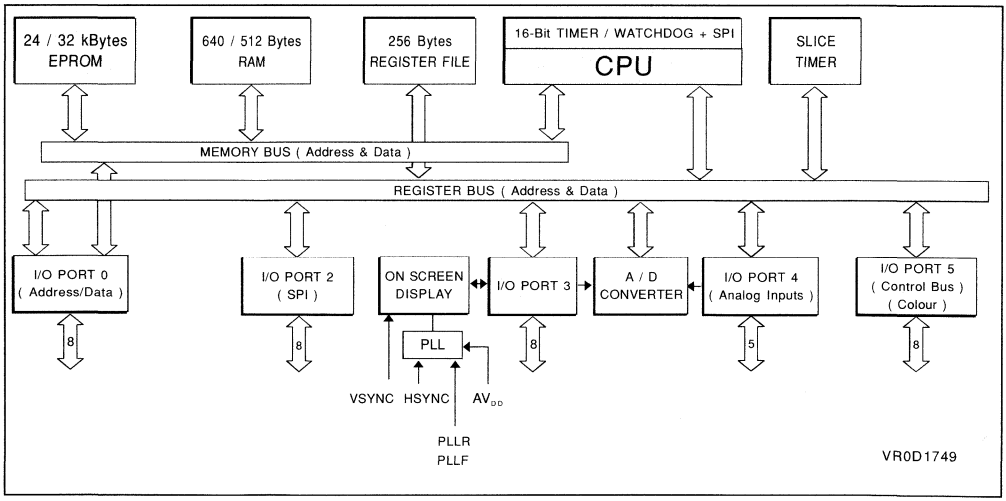
Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler and 6 operating modes allows simple use for waveform generation and measurement, PWM functions and many other system timing functions.

The human interface is provided by the On Screen Display module, this can produce up to 15 lines of of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

In addition there is a 4 channel Analog to Digital Converter with integral sample and hold, fast 5.5µs conversion time and 6-bit guaranteed resolution.

Figure 1. ST92E93 Block Diagram



DEVELOPMENTS TOOLS

SGS-THOMSON MICROELECTRONICS

ST9 STARTER KIT

EVALUATION KIT FOR ST9 MCU FAMILY

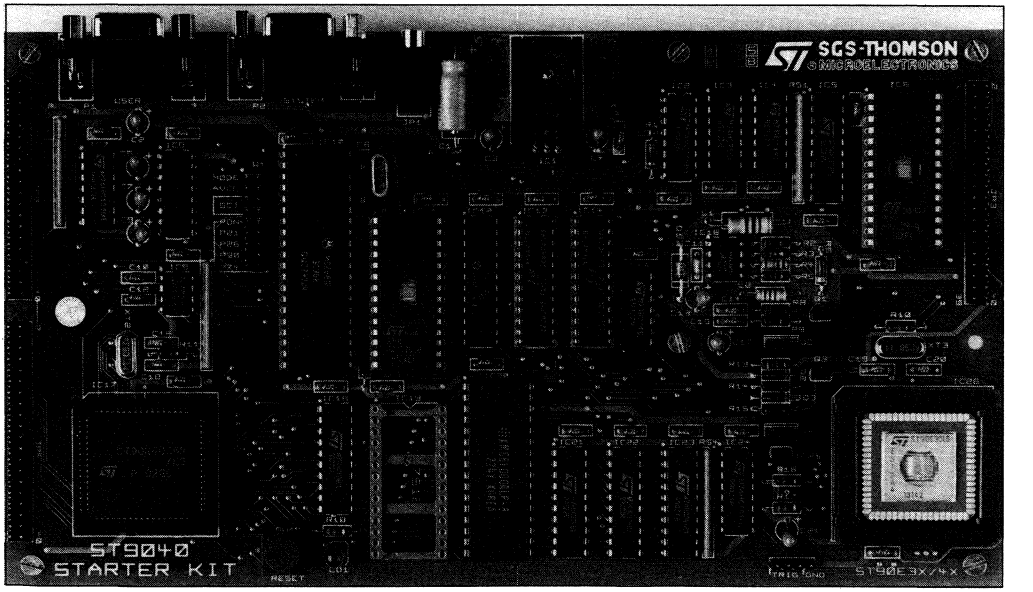
- Full Evaluation Kit for ST9 Family
- Emulation Capability
- Windowed and Command Line interfaces

GENERAL DESCRIPTION

The ST9 Starter Kit includes all the hardware, software and documentation required to evaluate the ST9 family of 8/16-bit MCUs and to develop simple applications. The ST9 Starter Kit includes ROMless (ST90R40) and EPROM-based (ST90E40) microcontrollers, the ST9 family documentation, the ST9 software tools package and an evaluation board for debugging an application and programming the ST90E40.

The board, which measures 225 x 125mm, is based on the ST90R40, which offers all the most important features of the ST9 family, including a built-in DMA controller, a Serial Peripheral Interface (supporting S-bus, I^2C-bus and IM-bus), 256 bytes of internal RAM, 512 bytes of internal EEPROM, 16-bit multifunction timers, A/D converter and a full duplex serial communication interface. On-board memories provide storage for emulated programs and data, the monitor program and breakpoint information.

For maximum flexibility, the board can run in three different modes. In the stand-alone mode, up to 64Kbytes of program space and 64Kbytes of data space are available. In the emulation mode, the board is driven by a monitor program allowing the use of all registers and memories, while single step, software trace and breakpoints are supported on both program and data spaces through debugging software running on a PC host. The third mode is the programming mode, which allows debugged software to be downloaded to an ST90E40 using the ZIF socket provided.



SOFTWARE TOOLS

The software tools include a full macro-assembler which supports modular programming, an incremental linker, an archiver that manages relocatable objects modules, a functional simulator, a windowed debugger which drives the ST9 evaluation board and the EPROM programming software. The fully symbolic debugger allows access to all ST9 resources (memories, registers) while the windowed and menu-driven interface, on-line help and intuitive access to commands make it very easy to use.

The ST9 Starter Kit also includes full documentation on the ST9040 Family, on how to connect and program it and the software tools manuals which describe how to use the ST9 development tools included in the starter kit, as well as a floppy disk containing several application programs for ST9 devices.

Starter Kit Command Line Summary

COMMAND	DESCRIPTION
ARchive	Archive symbols and macros
ASm	On-line Assembler
BAse	Change base of numbers
BYE	Exit from debugger program
CLOSE	Close I/O Channel
CLS	Clear screen
CM	Compare memory
DEfine	Define symbols and macros
DIsasm	On-Line disassembler
DM	Display memory
DO	Execute macro
DR	Display register
DUmp	Save current setup
ENDFOR	End for loop (see FOR)
ENDIF	End conditional block (see IF)
FM	Fill memory with pattern
FOR	Loop command execution
FR	Fill registers with pattern
GO	Execute program
Help	On-Line help
IF	Conditional command execution
JUMP	Go to label
LIstsymbol	List symbols and macros
LOad	Load program from file
LOCATE	Set cursor position at given coords
MAP	Set/Display mapping
MB	Modify memory breakpoints settings
MM	Move memory block
NEXT	Execute program steps

Starter Kit Command Line Summary (Continued)

OPEN	Open I/O channel
PAUSE	Pause for number of seconds
Print	Print strings and values
Quit	Return to Graphical Interface
REset	Reset emulated CPU
SAve	Save memory contents to file
SB	Set/Display memory breakpoints
SEarch	Search for pattern in memory
SET	Set/Reset emulator options
SM	Set memory
SR	Set/Display registers
SYstem	Exit temporarily to operating system
Trace	Display trace
UNdefine	Remove symbols
USE	Execute command file
VER	Print version information
WAtch	Display/Create watch data
WR	Display current working register set
<value>	Evaluate expression
!	Execute single system command
?	Display symbols having a given value
:	Comment line for macros/command files

SGS-THOMSON MICROELECTRONICS

ST9-GNU TOOLCHAIN

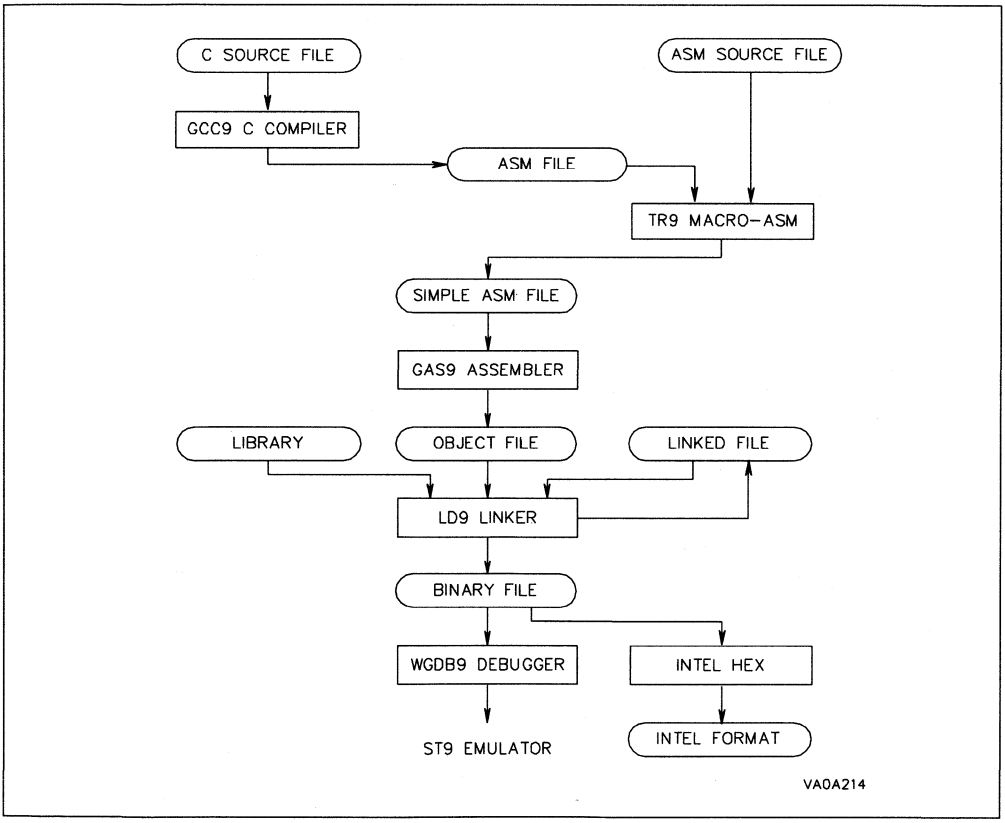
C COMPILER, ASSEMBLER, LINKER AND SOURCE DEBUGGER FOR ST9 MCU FAMILY

CONTENTS

- Optimised C compiler with options for different standards: traditional C, ANSI C, and GNU extensions
- Macro-assembler with powerful pre-processor
- Linker/loader
- Source-level debugger with Microsoft WINDOWS 3™ graphic interface
- Available for SUN 4 (SPARC STATION) under the UNIX system

GENERAL DESCRIPTION

The GNU Toolchain offers the software developer a full set of resources for the development of code for the ST9 microcontroller. This is achieved through the optimised GNU C Compiler, the Macro-assembler, Linker/Loader and Library Archiver. The Assembler is fully compatible at source level with previous version of the ST9 Assembler. Program debugging is made easier with the C Language Source Level Debugger, which runs under MSDOS or Microsoft Windows 3™ .



GNU C COMPILER

- All standard types allowed (char, int, short, long, signed or unsigned, float, and double) with Float types respecting the IEEE 754 standard
- Libraries delivered include string handling, conversion, I/O routines and mathematics
- Direct access to the Register File of the ST9, allowing access to all registers and on-chip peripherals
- Allows inclusion of assembly language instructions, with access to C program symbols
- Options to generate code for one or two memory spaces, one or two stacks and interrupt routines
- Optimisation phase included at final stage

General Description

The GNU C Compiler for the ST9 allows the programmer to write C source code (using traditional C (Kernigan & Richie), ANSI C, or GNU Extensions) and to produce assembly language source code. When used with the Assembler and Linker, it allows the generation of executable object code for all members of the ST9 family.

The generated assembly source file may include interleaved C lines and assembly language lines, and provides information for source-level debugging.

ASSEMBLER

The Assembler pre-processor allows macro substitution, file inclusion and conditional assembly and is fully compatible at source level with the ST9 assembler (AST9) pseudo-instructions and pseudo-macros.

Source level debugging information is generated with the object file by the assembler.

Assembly language programs are fully mixable with C language programs and accept 3 sections (TEXT, DATA, BSS).

LINKER

- Combines object code files issued by the assembler
- Supports incremental linking

General Description

The Linker resolves references to external symbols and searches libraries for necessary modules to produce an output file in a binary format, downloadable by the debugger to the ST9 emulator.

A map file is generated, including all mapping information on sections, files, and symbols and separate files are produced to support ST9 bank switch mechanism

The three sections generated by the C compiler and used by the assembler are accepted.

Options are available for setting the base addresses of sections and stacks and management of two spaces with script files to define memory mapping.

DEBUGGER

- Runs on MS-DOS based PC, with or without WINDOWS 3™
- Connected by serial line to the ST9 hardware emulator
- Offers a WINDOWS 3™ - based graphic interface, supporting all standard features
- Mouse supports access to context sensitive help
- Offers a line mode command interface (able to run on MS-DOS or within a WINDOWS 3™ DOS box) supporting command files
- Includes a window for access to the low-level SDBST9 debugger
- Dumps ST9 memories, system registers, Register File and paged registers

General Description

The ST9 Debugger allows source level debug for C language and assembly language programs, even with optimized C language programs.

The debugger is able to generate trace information, with hardware information interleaved with source lines, and to display the local symbols of the current C procedure and the stack based on the C language source level.

Source lines are displayed, with or without disassembly of memory interleaved with the source lines with symbols under their real types.

Requires 386 class PC or higher with at least 4 Mbytes of memory, under MS-DOS 4.01 or higher.

UTILITIES

- Archiver
- Formatter of INTEL HEX industrial format, allowing download of program to an EPROM programmer
- Binary file deformatter

Note: Windows 3 is a trademark of the Microsoft Corporation.

SGS-THOMSON MICROELECTRONICS

ST9-EPB

EPROM PROGRAMMING BOARD FOR ST9 MCU FAMILY

- Programming tool for EPROM and OTP members of the ST9 Microcontroller Family
- Stand-alone operation mode
- Device EPROM capacity self-identified
- 3 functions performed
- All device packages type supported
- Single Power Supply

GENERAL DESCRIPTION

This board is designed for programming the EPROM versions of the ST9 microcontroller family, including both the ceramic windowed and plastic OTP packages.

The EPROM size of the ST9 microcontroller to be programmed is recognised automatically by the on-board software and three sockets are provided to accept the different existing packages types.

The ST9-EPB board uses a reference EPROM including the customer's code directly generated by the ST9 assembler-linker. The ST9 EPROM device will be programmed from the contents of the reference EPROM. Jumpers allow the selection of different types of reference EPROM (2732, 2764, 27128, 27256).

On board regulation requires only a single power supply of +18 V_{DC} – 0.5A to produce the different voltages necessary for the board functioning.

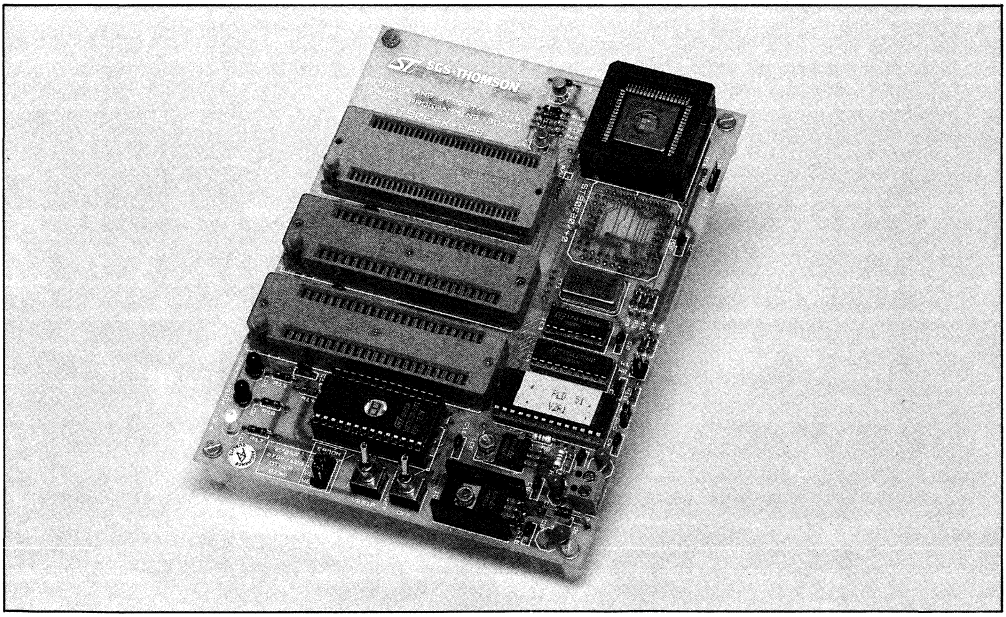
The board can perform 3 operations:

- Verifying the blank state of the microcontroller EPROM.
- Programming microcontroller with the content of the reference EPROM.
- Verifying the microcontroller against the reference EPROM.

The required function is selected by two switches.

During the running procedure the program/verify LED flashes and at the end of operation, the result is displayed on LEDs:

- Green OK LED for succesful operation.
- Red error LED for a programming error.



SGS-THOMSON MICROELECTRONICS

ST9-HDS

HARDWARE DEVELOPMENT SYSTEM FOR ST9 MCU FAMILY

- Designed to communicate with any IBM PC/XT/AT or compatible computer through an RS-232 serial communication link.
- Emulation capability of all present and future members of the ST9 Microcontroller family, ROM and ROMless devices by dedicated option boards
- 128K bytes of system mappable fast static memory, which may be mapped in pages of 512 bytes each
- 4 maskable hardware controlled memory breakpoints and 2 maskable hardware controlled register breakpoints
- Real time trace memory (2048 events)
- Programmable crystal oscillator and external clock option allow an emulated CPU clock frequency ranging from 2 to 24 MHz
- Automatic hardware self test executed every time the emulator is powered on
- 8 User Probes available and included in the trace and breakpoint logic
- The Emulator may be used in Standalone Mode without a Personal Computer control

GENERAL DESCRIPTION

The ST9 Hardware Development System (ST9-HDS) is an intelligent and powerful In Circuit Real Time Emulation System configurable for all current and future members of the ST9 family of microcontrollers. The complete ST9-HDS consists of the emulator, an RS232 Serial Communication Cable providing the interface with an optional Host computer, an ICE Probe and Adapter which may be plugged directly into the user's application, a set of 8 user probes, and a powerful software debugger. The ST9-HDS allows the designer to emulate the system in real time or single step mode. A set of 4 user programmable memory breakpoints which may be logically combined in AND, OR, SEQUENTIAL, or DELAY mode and 2 user programmable register breakpoints allow the user to stop emulation upon very specific conditions, while trace circuitry will collect the latest 2K (by 40 bit) events. Furthermore, a wide range of debug commands provides the user with full control of the Emulator hardware and features several commands for controlling the execution of programs. Memory and registers may be read and written in a number of different formats, while macro commands and conditional block constructs are available for use in automated debugging sessions.

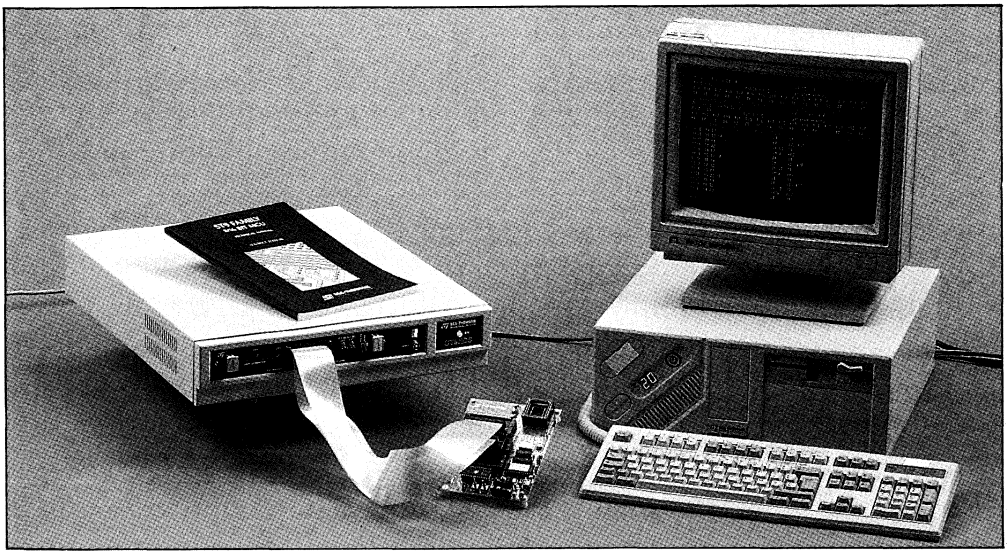
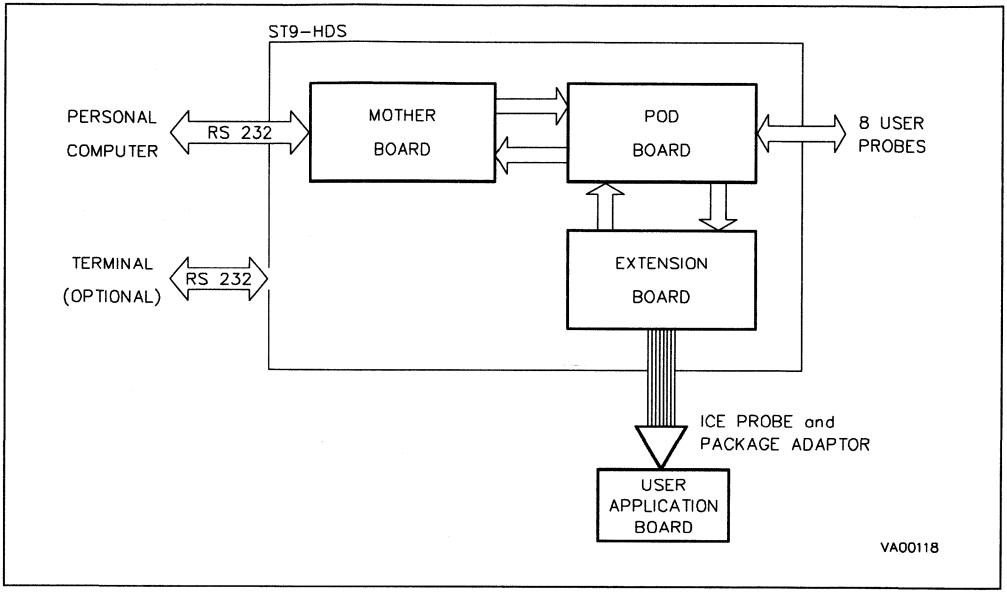


Figure 1. ST9-HDS System Configuration



HARDWARE DESCRIPTION

The Interface and Control Unit (ICU) contains most of the circuitry necessary to control the ST9-HDS, with the exception of the circuits specifically related to the ST9 family of microcontrollers. The ICU provides the control logic for monitoring the execution of programs, setting memory breakpoints, recording signal events, and handling the communication with the host computer. The board contains the following hardware resources:

- Private Microcontroller: A private microcontroller controls the operation of the emulator, allowing execution of an emulated program to run without interference.
- 128K of Fast Static Memory: 128 Kbytes of fast static memory are available for use by the emulated microcontroller.
- Memory Management Circuitry: Memory may be mapped in groups of 512 bytes as Internal/External to the Emulated ST9 or, System/User Supplied, and ReadOnly/ReadWrite, or as Non Existent. (Certain versions also allow memory to be mapped as EEPROM memory.)
- Memory Breakpoints: 4 Hardware controlled memory breakpoints are available to the user and may be combined in AND, OR, SEQUENTIAL, or DELAY mode. Each of the four breakpoints is associated with a breakpoint counter which may be used simply as a counter or used to flag an event only after the associated event has occurred n times.
- Real Time Trace Circuitry: Real Time Trace Circuitry keeps track of a 2K by 40 bit buffer.

The ST9 Emulator POD contains the core of the circuits required to emulate any member of the ST9 family of microcontrollers. This board is responsible for providing the interface with the Extension Board, providing the interface with the Interface Control Unit, sending out signals on reset identifying the emulated device as a ROM-less or ROM-maskable device, managing the opcode fetch signals, generating the clock for the Extension Board, controlling the standalone mode option, decoding the pod addresses, managing the register breakpoints, controlling the idle/run logic, generating wait cycles, and accessing the 8 user probes. The Pod Board contains the following features:

- Programmable Crystal Oscillator: An on board programmable crystal oscillator, as well as the possibility of using an external clock via a BNC connector, allow the user the option of selecting the emulated CPU clock frequency.
- Standalone Logic: The Hardware Development System may be operated in Standalone Mode, that is independently of the Host computer.
- Wait Cycle Generator: A Wait Cycle Generator allows the user to assign from 0 to 7 wait cycles to any block of 512 memory bytes defined as external.

HARDWARE DESCRIPTION (Continued)

- Register Breakpoints: 2 Hardware controlled register breakpoints are available to the user and may be combined in AND or OR mode.

The Extension Board contains the circuitry controlling all the special functions and peripherals of the ST9 being emulated. Since each version of the ST9 has different peripherals and access to different I/O ports, the Extension Board will be different for each version of the ST9.

However, the basic design of the Extension Board will remain the same, allowing the extension board to be easily configured for any future or existing version of the ST9. In general, the Extension Board contains the components and circuitry which emulate the ST9 (Core, I/O ports, and peripherals), interfaces with the ICE Connectors, and sends information to the Pod Board. Either a 220V/50Hz or 110V/60Hz Power Supply is included in the emulator to provide the emulator with all necessary power.

SOFTWARE DEBUGGING PACKAGE

The ST9 Symbolic Debugger is a software tool which allows the user to have complete control of the ST9 Hardware Development System. The Debugger must be used on an IBM PC/XT/AT or compatible that is connected to the ST9-HDS by means of an RS-232 serial communication cable. The following features are provided by the ST9 Symbolic Debugger:

- Debugger Compatibility: The debugger has a command line syntax compatible with the SIMST9 Software Simulator and SDBST9, the debugger for the ST9 Evaluation Module.
- Commands: A wide range of commands are available for displaying and setting memory and registers according to different formats.
- Powerful Symbol Handler: A Powerful Symbol Handler allows the user to define symbols and macros, extract them from symbol table files, and save them in symbol table files.
- Symbolic On-Line Assembler/Disassembler: The debugger provides a symbolic on-line assembler and disassembler.
- Full Screen Video Mode: Full screen video modes are available for Memory, Register, and Single Step Display.
- Symbolic Trace: Trace memory is disassembled into assembler mnemonics.
- Macros and Conditional Block Constructs: Macro commands and conditional block constructs are available for use in automated debugging sessions.
- On-Line Help: An On-line help facility is available in the debugger to give a listing of the complete command set as well as specific information on any of the commands.
- Configuration and Documentation: Log, dump and command file capability allows for easy documentation and configuration.
- Powerful Command Interpreter: A powerful command interpreter allows for the evaluation of complex expressions involving numbers, addresses, memory and register contents, and I/O channel data.

The ST9 Symbolic Debugger accepts inputs from the Software Development Package which includes the following:

- ST9 Macro Assembler (AST9)
- ST9 Linker/Loader (LST9)
- ST9 Library Archiver (ARST9)
- ST9 Software Simulator (SIMST9)

The Software Development Package is available separately, or with the Hardware Development System.

Figure 2. SDBST9 Command Summary

ARCHIVE	Archive symbols and macros
ASM	On-line assembler
BASE	Change base of numbers
BYE	Exit from debugger program
CLOSE	Close I/O channel
CM	Compare memory
DEFINE	Define symbols and macros
DISASM	On-line symbolic disassembler
DM	Display memory
DO	Execute macro
DR	Display register
DUMP	Save current setup
FM	Fill memory
FR	Fill registers
GO	Execute program
HELP	On-line help
IF	Conditional command execution
LISTSYMBOL	List symbols and macros
LOAD	Load program/data from file
MAP	Set/display memory mapping
MB	Modify breakpoint
MM	Move block of memory
MRB	Modify register breakpoint
NEXT	Execute program steps
OPEN	Open I/O channel
PRINT	Print strings and values
QUIT	Terminate command execution
RESET	Reset emulated CPU
SAVE	Save program/data into file
SB	Set/display memory breakpoints
SEARCH	Search a pattern in memory
SET	Set/reset options
SM	Set memory
SR	Set/display registers
SRB	Set/display register breakpoints
TRACE	Display trace
UNDEFINE	Remove symbols
USE	Execute commands from a file
VE	View execution (video mode)
VM	View memory (video mode)
VR	View registers (video mode)
WR	Display current working register set
<value>	Evaluate expression
?	Display symbols having a given value

SOFTWARE DEVELOPMENT TOOLS FOR ST9 MCU FAMILY

- ST9 Macro Assembler
- ST9 Linker/Loader
- ST9 Library Archiver
- ST9 Software Simulation

GENERAL DESCRIPTION

Full software development is achieved using the ST9 Software Development Tools. This follows for the optional C Compiler, through the High Level Macro Assembler, Linker/Loader, Library Archiver and Software Simulator.

ST9 Macro Assembler

The ST9 Macro Assembler accepts one or more source files written in ST9 assembly language and transforms them into linkable object files. The assembler recognizes the use of symbols, macros, pseudo-instructions, pseudo-macros, and conditional assembly directives.

ST9 Linker/Loader

The ST9 Linker/Loader combines a number of object files into a single program, associating an absolute address to each section of code, and resolving any external references. LST9 may be used to generate: a binary or hexadecimal output module, a map file, and an object file.

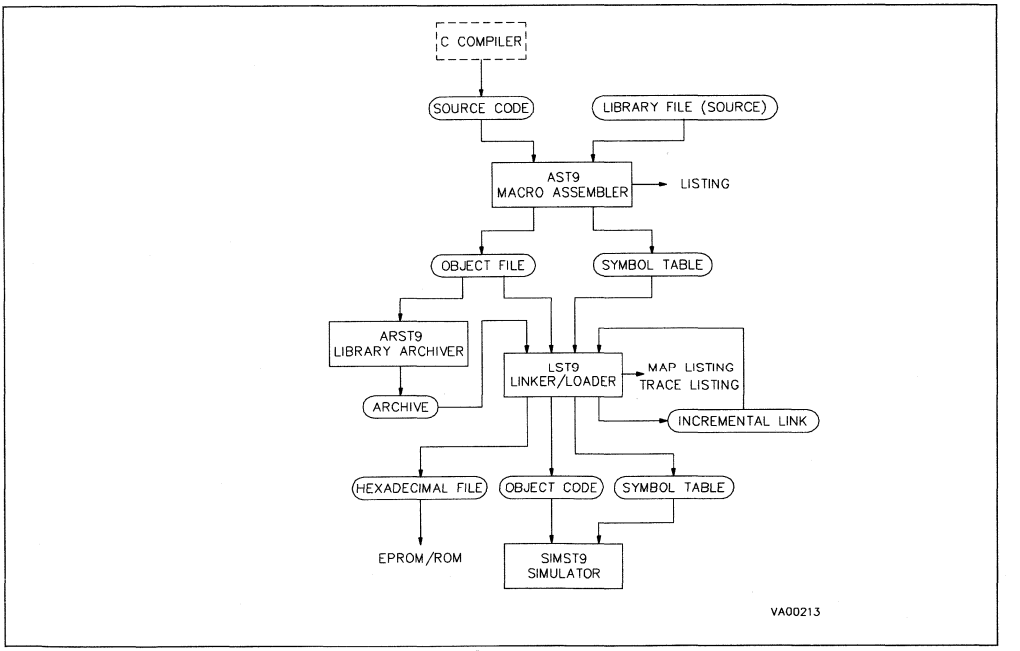
ST9 Library Archiver

The ST9 Library Archiver maintains libraries of software object files, allowing the user to develop standard modules for repetitive use.

ST9 Software Simulator

The ST9 Software Simulator allows the user to debug and execute any program written for any member of the ST9 family of microncontrollers without the aid of additional hardware. The simulator functionally duplicates the operation of the ST9 and completely supports the instruction set.

Figure 1. Development Flow Chart



AST9 - ST9 MACRO ASSEMBLER

- Accepts one or more source files written in ST9 assembly language and produces an object file, a listing file, an alphabetical symbol table, and error diagnostics
- Resulting object files are linkable and relocatable
- Supports program segmenting directives
- Recognizes user defined macros, macro libraries, Conditional assembly directives, pseudo-instructions, and pseudo-macros
- Supports indirect command files

General Description

The ST9 Macro Assembler (AST9) accepts one or more source files written in ST9 assembly language and transforms them into linkable object files. Modules written in assembly language are much easier to write, read, and debug than the equivalent machine code. Furthermore, the assemblers use of symbols, macros, pseudo-instructions, pseudo-macros, and conditional assembly directives, allows for even easier program development.

Figure 2. AST9 Pseudo-Instructions

```
.ascii      stores a string as a sequence of ascii codes
.asciz      same as above followed by a null character
.blkb       allocate bytes of data storage
.blkw       allocate words of data storage
.bss        defines segment as type bss (uninitialized data)
.byte       stores successive bytes of data
.data       defines segment as type data
.defstr     defines a string identifier
.endc       end of a conditional assembly block
.endm       end of a macro
.error      user defined assembly error
.extern     defines symbols as external
.global     defines specified symbols as global
.ifc        beginning of a conditional assembly block
.library    add files to macro-library file list
.list       enables listing of specified fields
.macro      defines a macro
.mcall      specifies which macros must be called from library
.mnarg      assigns to a symbol the number of arguments
            defined in a macro call
.mexit      end of a macro expansion
.nlist      disables listing of specified fields
.org        set current location counter
.page       start a new listing page
.pl         set listing page length
.sbttl      assign subtitle to current section
.text       define segment of type text
.title      assign title to the document
.word       store successive words of data
```

AST9 - ST9 MACRO ASSEMBLER (Continued)

Figure 3. AST9 Pseudo Macros

```
jxcc symbol
if [conditional expression] {macrobody}
if [cond expr] {macrobody} else {macro2}
while [cond expr] {macro}
do {macro} while [cond expr]
loop [loopvar] {macro}
switch [cp] {
        case cp1: macro
        case cp2: macro
        default: macro
}
break
begin [arg1,arg2,...] {macro}
proc procname [arg1,arg2,...] {macro}
return
```

LST9 - ST9 LINKER/LOADER

- Links modules generated by the ST9 Macro Assembler (AST9) encourages modular programming
- Supports indirect command files
- Supports 3 sections (text, data, and bss) which may be relocated and loaded at different addresses. Allows the user to specify the mapping of object files into different pages (supports 8Mbyte addressing of the ST9050).
- Extensive symbol manipulation. produces alphabetically or numerically sorted symbol tables for addresses, registers, or specifically for SIMST9 and SDBST9, strips the symbol table of local symbols, global symbols, or both, allows definition and tracing of symbols.
- Produces binary or hexadecimal output modules
- Generates a map file
- Supports incremental linking
- Resolves references to external symbols and searches libraries for necessary modules
- Provides self explanatory error and warning messages.
- Displays the version number and information about the various phases of linking

General Description

The ST9 Linker/Loader (LST9) is responsible for combining a number of object files into a single program, associating an absolute address to each section of code, and resolving any external references.

LST9 can be used to create either a binary or hexadecimal output module to be used by the ST9. The linker/loader will also produce a map file of the resulting object which gives information about the registers, pages, modules, and labels, or an object file which may be used as an input to another call to the linker.

This software program allows the user to develop modular programs, which may then be combined and addressed as defined by the user. Program modularity allows for easier design and testing, as well as promotes re-use of standard modules.

ARST9 - ST9 LIBRARY ARCHIVER

- Edits libraries by adding, deleting, moving, or replacing files
- Prints a listing of the names of all files in a library, or the table of contents for each file in a library
- Prints a file contained in a library, or extracts it for use without modifying the library
- Libraries may be called by LST9 to resolve external references.

General Description

The ST9 Library Archiver (ARST9) maintains libraries of software object files, allowing the user to develop standard modules for repetitive use. Once a module has been inserted into a library, any application may call the module. The ST9 Linker/Loader (LST9) will only call the portions of each library that are needed to resolve any external references.

SIMST9 - ST9 SOFTWARE SIMULATOR

- Supports symbolic debugging and execution of any program written for the ST9 family of microcontrollers on an IBM PC/XT/AT or compatible computer, without the aid of additional hardware.
- Functionally duplicates the operation of the ST9 family of microcontrollers, and supports the complete instruction set.
- Host Memory may be mapped in groups of 1K byte as Read-only, Read-write, or Non Existent.
- A series of simulator status commands give the user the option of selecting the simulated CPU clock frequency, creating a log of the simulator session, tracing the executed instructions, or enabling the breakpoints and traps.
- The simulator has a command line syntax compatible with SDBST9, the debugger for the ST9-HDS Hardware Development System, and EVMST9, the debugger for the ST9-EVM Evaluation Module.
- A powerful symbol handler allows the user to define symbols and macros, extract them from symbol table files, and save them in symbol table files.
- Full screen video modes are available for Memory, Register, and Single Step Display.

SIMST9 - ST9 SOFTWARE SIMULATOR (Continued)

- An On-line help facility is available to give a listing of the complete command set as well as specific information on any of the commands.
- Dump and command file capability allow for simulator session retrieval and easy configuration.
- The simulator provides a symbolic on-line assembler and disassembler.
- A powerful command interpreter allows for the evaluation of complex expressions involving numbers, addresses, memory and register contents, and I/O channel data.
- 128 software breakpoints and 128 software traps are available to the user.
- A trace is kept during program execution which may be displayed afterwards with the traced instructions disassembled into assembler mnemonics.
- A wide range of commands are available for displaying and setting memory and registers according to different formats.
- Macro commands and conditional block constructs are available for use in automated debugging sessions.
- I/O channels can be opened for simulation of I/O peripheral functions.
- Interrupts may be defined and set pending to simulate the occurrence of an interrupt.
- A simulated clock will use the user assigned clock frequency to calculate the real time execution of a program. The clock may be displayed or changed by the user to perform time measurements.

General Description

SIMST9 allows the user to debug and execute any program written for any of the current and future members of the ST9 family of microcontrollers, without the aid of additional hardware. The simulator functionally duplicates the operation of the ST9 and completely supports the instruction set. I/O channels may be opened, read, and written, in order to simulate the I/O functions of peripherals, while interrupts may be set, and then set pending, in order to simulate the handling of interrupts. The simulator uses the clock frequency assigned by the user, along with the number of clock cycles needed by each instruction to keep track of the real time execution speed.

Figure 4. SIMST9 Command Summary

```
ARCHIVE          Archive symbols and macros
ASM              On-line assembler
BASE             Change base of numbers
BYE              Exit from simulator program
CLOSE            Close I/O channel
CM               Compare memory
DEFINE           Define symbols and macros
DEFINT           Define Interrupts
DISASM           On-line symbolic disassembler
DM               Display memory
DO               Execute macro
DR               Display register
DUMP             Save simulator status
FM               Fill memory
FR               Fill registers
GO               Execute program
HELP             On-line help
IF               Conditional command execution
INTERRUPT        Simulate interrupt
```

Figure 4. SIMST9 Command Summary (Continued)

LISTSYMBOL	List symbols and macros
LOAD	Load program/data from file
MAP	Set/display memory mapping
MB	Modify breakpoint
MM	Move block of memory
MT	Modify trap
NEXT	Execute program steps
OPEN	Open I/O channel
PRINT	Print strings and values
QUIT	Terminate command execution
RESET	Reset simulated CPU
RESTORE	Restore dump file
SAVE	Save program/data into file
SB	Set/display memory breakpoints
SEARCH	Search a pattern in memory
SET	Set/reset options
SM	Set memory
SR	Set/display registers
ST	Set/display traps
TIME	Set/display user clock counter
TRACE	Display trace
UNDEFINE	Remove symbols
USE	Execute commands from a file
VE	View execution (video mode)
VM	View memory (video mode)
VR	View registers (video mode)
WR	Display current working register set
<value>	Evaluate expression
?	Display symbols having a given value

ST9-C

ANSI C COMPILER FOR ST9 MCU FAMILY

- Upgraded KERNIGHAN AND RITCHIE C definition, respecting ANSI standard X3.159.
- Optimisation stages using artificial intelligence techniques (calculation of costs in terms of code size and execution time).
- Versions available for IBM PC or compatible under MS-DOS 3.1 and higher, SUN 3 and SUN 4 (SPARC station) under the UNIX operating system and for VAX and microVax under the VMS operating system.
- All standard types allowed (char, int, short, long, signed or unsigned).
- "Float" respecting IEEE 754 standard and "Double" types allowed.
- Many library functions implemented in assembler code for increased code and execution time efficiency e.g. string handling, conversion, I/O routines.
- Generates an assembly language source file, interleaving C lines and assembly language lines.
- Direct access to the Register File of the ST9, allowing access to all on-chip peripherals and features of the ST9.
- Extensions for Real Time Interrupt handling.
- Pre-processor included for standardisation and increased readabilty and portability.
- Available with Macro-Assembler, Linker and Symbolic Software Simulator.
- Fully compatible with the ST9 Hardware Development System supporting symbolic debug and source code high-level debugger.

GENERAL DESCRIPTION

The ST9 ANSI C Compiler allows the programmer to write C source code and produce assembly langage source programs. Used with the assembler/linker, it allows the possibility to generate object code executable for all members of the ST9 microcontroller family. The generated object code may be used for symbolic debugging with the software simulator and hardware debugger/emulator, to generate test EPROM devices for prototyping, or to produce ROM mask data. It takes into account all the advanced features of the ST9 family (interrupt, Register File access, memory pages access). The high-level language C Compiler has been designed to provide the greatest flexibility of use.

The user can either run the complete software with only one simple command, or run each step of the compiler separately: pre-processor, analyser, coder, optimizer.

The ST9 ANSI C Compiler is delivered with a standard initialisation file to be linked with the customer application. This file allows the setting of BSS and DATA sections and stack pointers, as well as peripheral startup code.

STANDARD

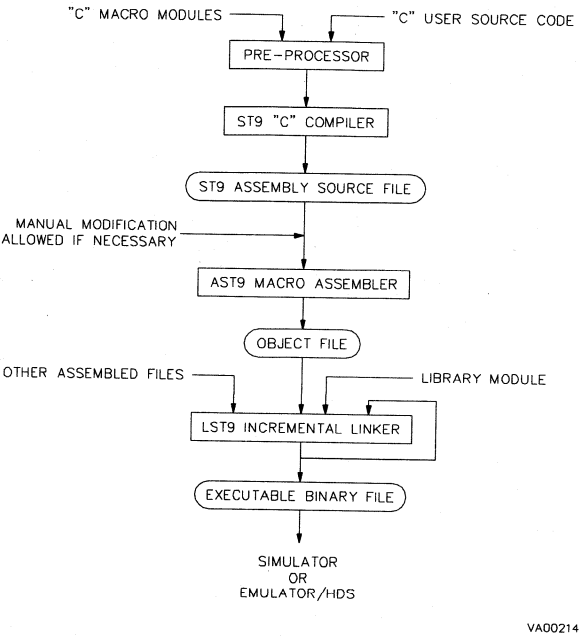
The ST9 ANSI C Compiler is an implementation of the X3.159 ANSI standard (issued from X3J11 draft proposal), which includes and exceeds the Kernighan and Ritchie specification. For example : "CONST" and "VOLATILE" qualifiers and function prototyping.

The ST9 ANSI C Compiler implements the features most often needed by microcontroller developments: interrupt handling, Register File access, far function declarations.

LICENSE

The ST9 ANSI C Compiler is delivered under license for one user only. Upgrading of new releases will be made to each registered user, free of charge, for a duration of 12 months starting from the date of the return of the Registration Card.

Figure 1. ST9-C Flow Chart



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